

09177-1M

Sheet

Sheet 1	COVER PAGE
Sheet 2	BLOCK DIAGRAM
Sheet 3	POWER DISTRIBUTION
Sheet 4	CLOCK DIAGRAM
Sheet 5	RESET MAP
Sheet 6	GPIO TABLE
Sheet 7	CPU HT INTERFACE
Sheet 8	CPU CNTL/STRAPS
Sheet 9	CPU MEM_A
Sheet 10	CPU MEM_B
Sheet 11	CPU POWER/GND
Sheet 12	CPU DECOUPLING
Sheet 13	MEM_DIMM_A0
Sheet 14	MEM_DIMM_B0
Sheet 15	MCP61 HT/CLKS
Sheet 16	MCP61 PEX X16
Sheet 17	MCP61 PEX X1/RGMII/HDMI/DAC
Sheet 18	MCP61 PCI/LPC
Sheet 19	MCP61 SATA/IDE
Sheet 20	MCP61 AUDIO/USB/MISC
Sheet 21	MCP61 PWR/GND
Sheet 22	MCP61 DECOUPLING/SPI
Sheet 23	HDMI CONNECTOR
Sheet 24	VGA CONNECTOR
Sheet 25	PCIEX16 CONNECTOR

Sheet

Sheet 26	PCIEX1 CONNECTOR
Sheet 27	VT6315N 1394 CONTROLLER
Sheet 28	USB+E-SATA CONNECTOR/FRONT
Sheet 29	USB+RJ45 CONNECOTR/FRONT
Sheet 30	LAN RTL8211CL/8201EL
Sheet 31	SIO IT8758E/DEBUG
Sheet 32	SERIAL PORT & KB, MS
Sheet 33	PARALLEL PORT/HEADER
Sheet 34	POWER SEQUENCING
Sheet 35	PWR/FNT PNL/SPKR/VBAT
Sheet 36	FAN CIRCUITS/HOLE
Sheet 37	AUDIO CODEC
Sheet 38	AUDIO CODEC JACKS
Sheet 39	DUAL RAIL VREG/1.1VSB
Sheet 40	NCP5393 CONTROL
Sheet 41	NCP5393 PHASE 1, 2, 3
Sheet 42	APW7120 1.1V
Sheet 43	APW7120 1.8V
Sheet 44	LDO FOR 2.5V/1.2V/0.9V
Sheet 45	EuP (Energy-using Products)
Sheet 46	PCI

<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Cover page			
Size A3	Document Number eMaguire	Rev 1M	
Date: Thursday, February 11, 2010 Sheet 1 of 46			

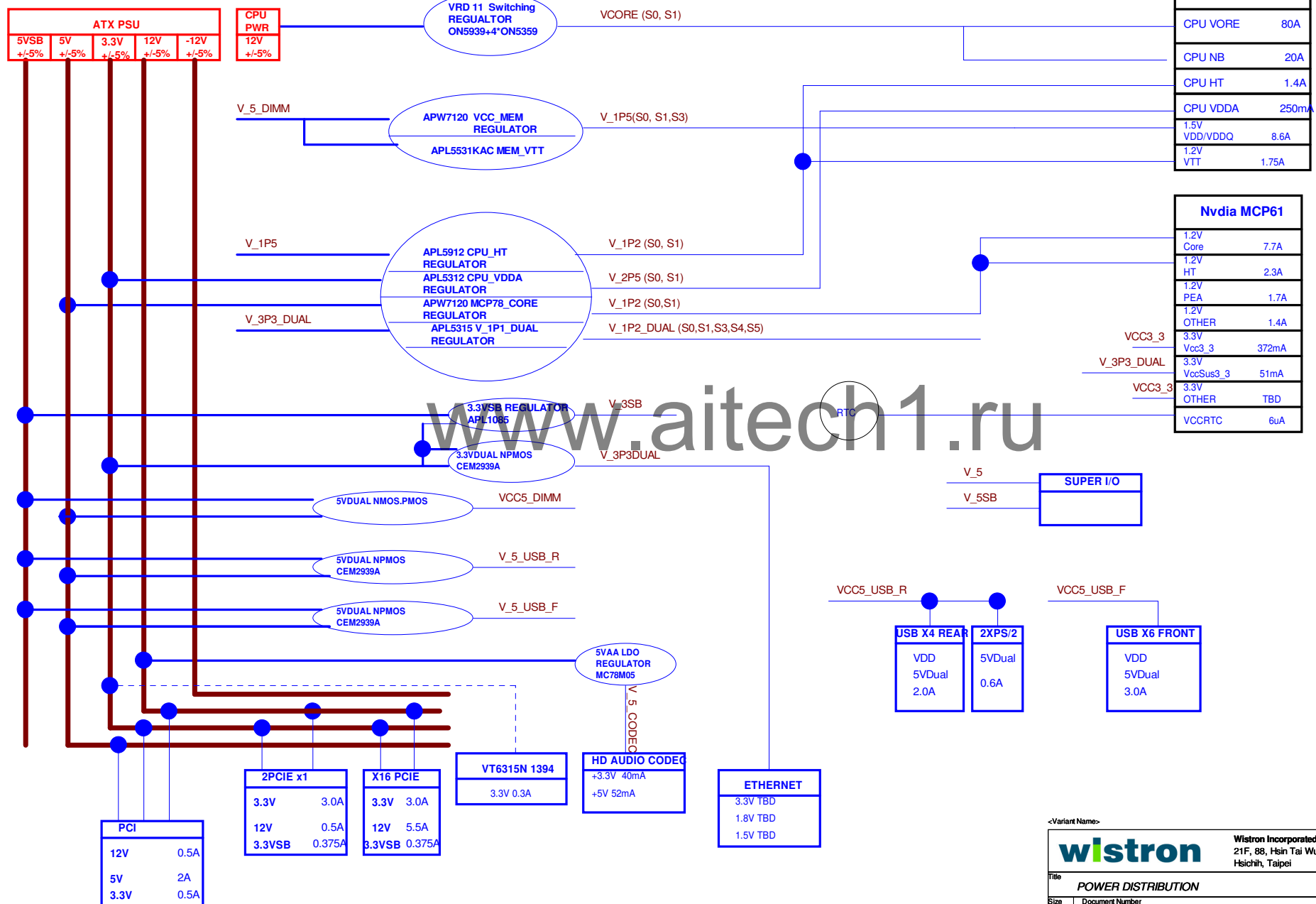
FRONT PANEL VIEW

- USB PORTS 2-3
- FRONT PANEL HDR
- USB PORTS 4-5



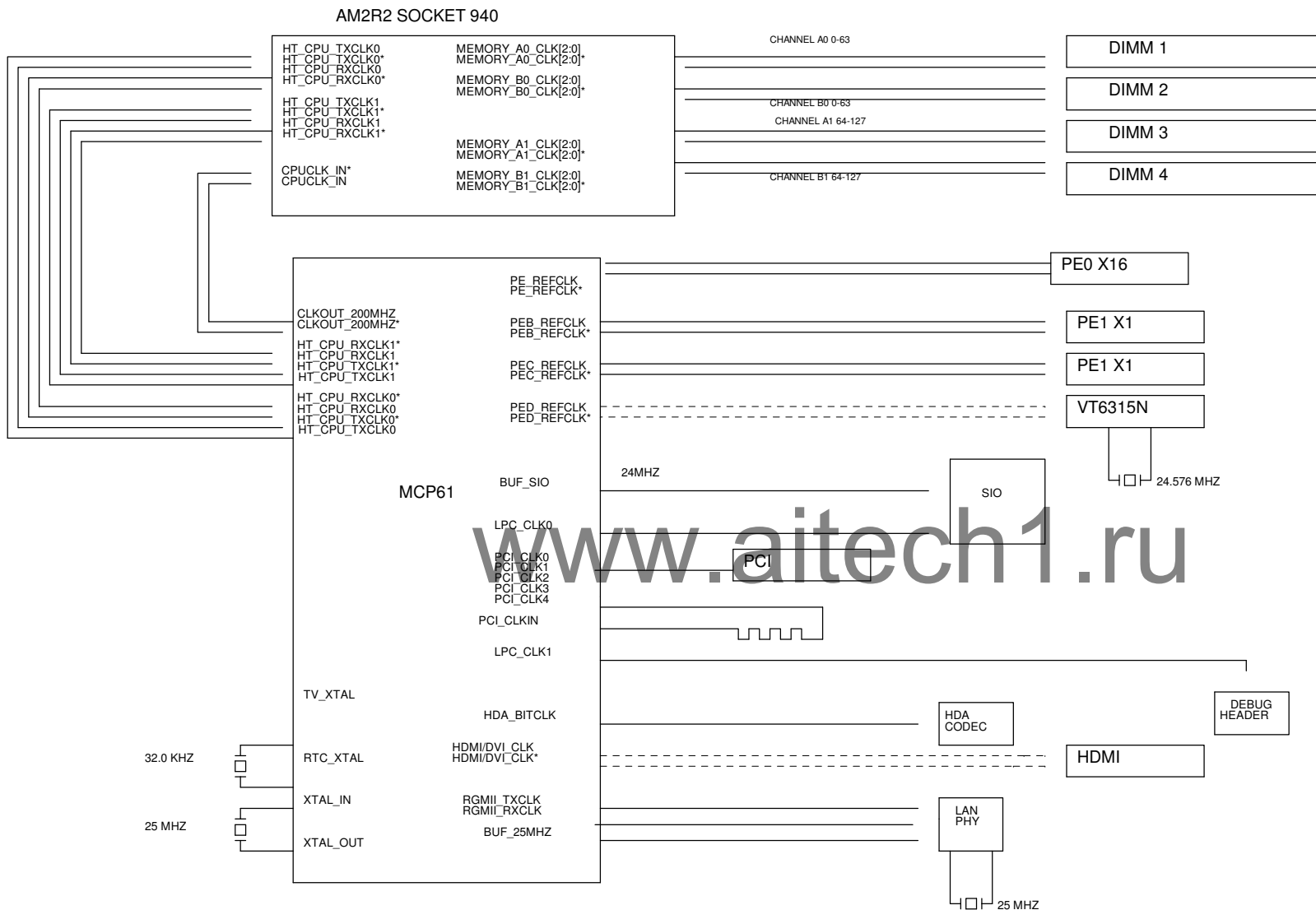
Total:	932
--------	-----

MCP61 Power Delivery Architecture




<Variant Name>

wistron			Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
POWER DISTRIBUTION			
Size	Document Number	Rev	
Customer	Maguire	1M	
Date:	Thursday, February 11, 2010	Sheet	3 of 46

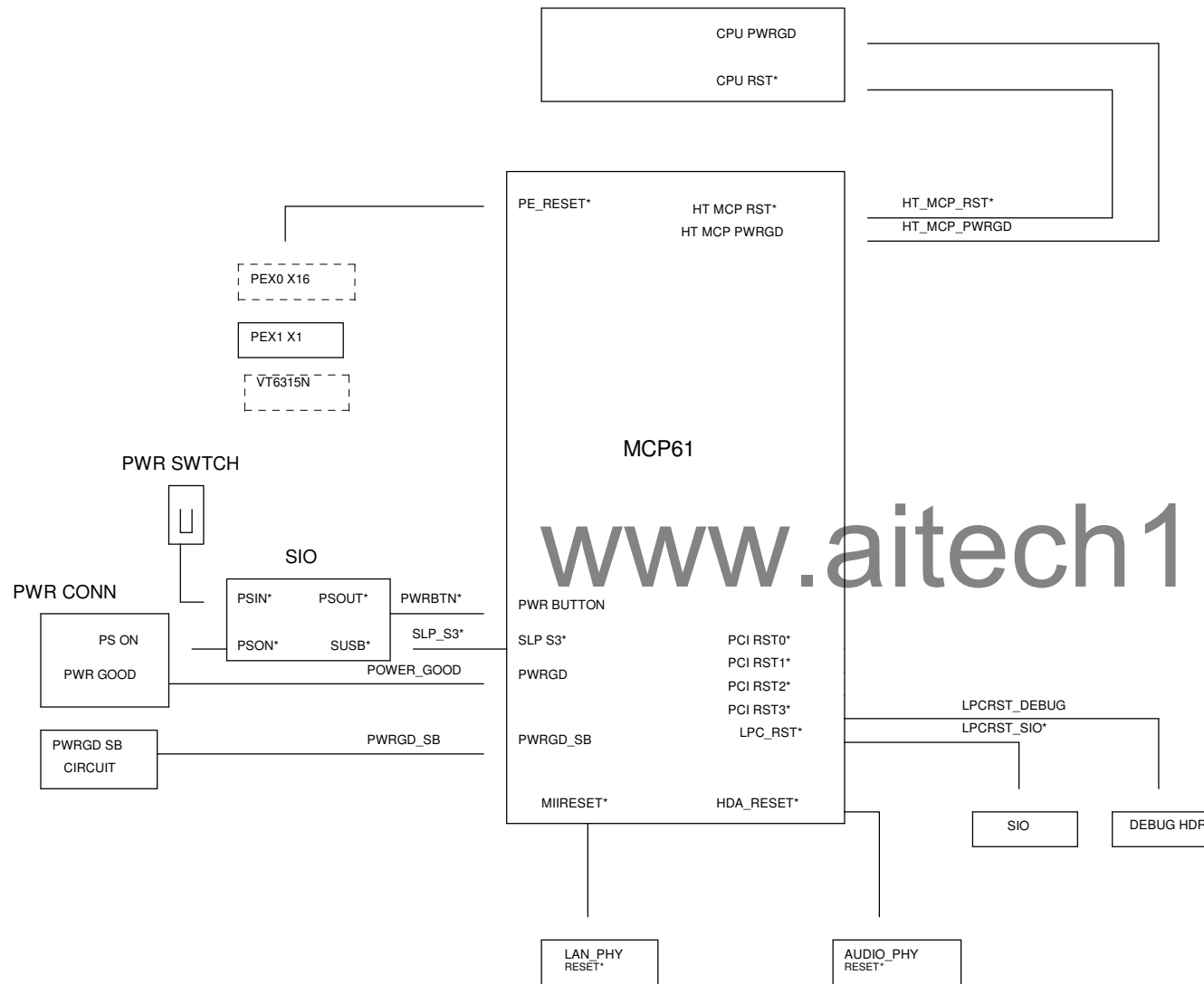


<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title CLOCK DIAGRAM			
Size A3	Document Number eMaguire	Rev 1M	
Date:	Thursday, February 11, 2010	Sheet	4 of 46

RESET MAP

AM3 SOCKET 941



<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page
Title	Author	Date	Page

RESET MAP

Size
A3

3	Document Number eMaquire
---	-----------------------------

Rev	
1M	

Date: Thursday, February 11, 2010

Sheet 5 of 46

SIO GPIO TABLE			
PIN NAME	ATTRIBUTE	POWER	FUNCTION
5 FAN_TAC2/ GP52	DI/ DIOD8	VCC	
6 FAN_CTL2/ GP51	DOD8/ DIOD8	VCC	
11 PECL_RQT/ GP14	PECV/ DIOD8	VCC	
12 PWROK1/ GP13	DOD8/ DIOD8	VCC	
13 PCIRST1#/ GP12	DOD8/ DIOD8	VCC	
14 PCIRST2#/ GP11	DOD8/ DIOD8	VCC	
24 KRST#/ GP62	DO16/ DIOD16	VCC	
33 PWRON#/ GP44	DOD8/ DIOD8	VCCH	
34 PME#/ GP54	DOD8/ DIOD8	VCCH	
35 PANSWH#/ GP43	DI/ DIOD8	VCCH	
36 PS0N#/ GP42	DOD8/ DIOD8	VCCH	
37 SUSC#/ GP53	DI/ DIOD8	VCCH	
38 3VSBSW#/ GP40	DO8/ DIOD8	VCCH	
39 KDAT/ GP61	DIOD24/ DIOD24	VCCH	
40 KCLK/ GP60	DIOD24/ DIOD24	VCCH	
41 MDAT/ GP57	MDAT/ GP57	VCCH	
42 MCLK/ GP56	FAN_TAC2/ GP52		
43 PCIRST3#/ GP10	FAN_TAC2/ GP52		
44 RSMRST#/ GP55	FAN_TAC2/ GP52		

MCP61 GPIO TABLE	
PIN NAME	FUNCTION
THERMTRIP*/GPIO58 PROCHOT*/GPIO20	CPU_THERMTRIP* CPU_PROCHOT*
MII0_RXER/GPIO36 MII0_COL/GPIO13/M2C_DATA MII0_CRS/GPIO14/M2C_CLK RGMII/MII0_INTR/GPIO35 RGMII/MII0_PWRDWN/GPIO37 MII0_RESET*	-- -- -- RGMII_INTR* RGMII_PWRDWN RGMII_RESET*
DDC_CLK0/3 DDC_DATA0/3	VGA/HDMI DDC_CLK VGA/HDMI DDC_DATA
PCI_REQ2*/GPIO40/RS232_DSR* PCI_REQ3*/GPIO38/RS232_CTS* PCI_REQ4*/GPIO52/RS232_SIN* PCI_GNT2*/GPIO41/RS232_DTR* PCI_GNT3*/GPIO39/RS232_RTS* PCI_GNT4*/GPIO53/RS232_SOUT* PCI_PERR*/GPIO43/RS232_DCD* PCI_PME*/GPIO30 LPC_PWRDWN*/GPIO54/EXT_NMI* LPC_DRQ0*/GPIO50 LPC_DRQ1*/GPIO15/FANRPM1	-- -- -- -- -- -- -- -- LPC_DRQ0* --
CABLE_DET_P/GPIO63 SATA_LED*/GPIO57	-- SATA_LED*
HDA_SDATA_OUT0/GPIO45 HDA_SDATA_IN0/GPIO22 HDA_SDATA_IN1/GPIO23/MGPIO0 HDA_SDATA_IN2/GPIO24 HDA_SYNC/GPIO44 GPIO_1/PWRDN_OK/SPL_CS1 GPIO_2/NMI*/PS2_CLK0* GPIO_3/SMI*/PS2_DATA0* GPIO_4/SCI_INTR/PS2_CLK1* GPIO_5/NMI*/PS2_DATA1* GPIO_6/FERR*/SYS_FERR*/GPU_GPIO_6* GPIO_7/NFERR*/SYS_FERR*/GPU_GPIO_7* GPIO_8/SPL_DI* GPIO_9/SPL_DO* GPIO_10/SPL_CS GPIO_11/SPL_CLK USB_OC0*/GPIO25 USB_OC1*/GPIO26 USB_OC2*/GPIO27 USB_OC3*/GPIO28/MGPIO_1 USB_OC4*/GPIO29 A20GATE/FANCTL3/GPIO55 EXT_SMI*/GPIO32 RI*/GPIO33 SIO_PME*/GPIO31/SPL_CS2 KBRDRSTN*/FANRPM3/GPIO56 SUS_CLK/GPIO34 THERM*/GPIO59 FANRPM0/GPIO60 FANCTL0/GPIO61 FANCTL1/GPIO62 THERM_SIC/GPIO48 THERM_SID0/GPIO49 THERM_ALERT*/PWR_LED/GPIO47 PE_WAKE*/GPIO21	HDA_SDATA_OUT HDA_SDATA_IN0 -- HDA_SYNC -- -- -- DEBUG_INTR -- -- SPL_DI* SPL_DO SPL_CS SPL_CLK USB_OC_10* USB_OC_32* USB_OC_54* USB_OC_76* USB_OC_98* A20GATE EXT_SMI* SER_RI* IO_PME* SIO_KBRST* -- CPU_THERM* -- -- THERM_SIC THERM_SID CPU_THERM_ALERT* PE_WAKE*

JUMPER SETTING

Location	FUNCTION	1-2	2-3
JBIOS1	CMOS	NORMAL*	CLEAR

* DEFAULT SETTING


B:For MCP78
E:For MCP61

L: without spdif

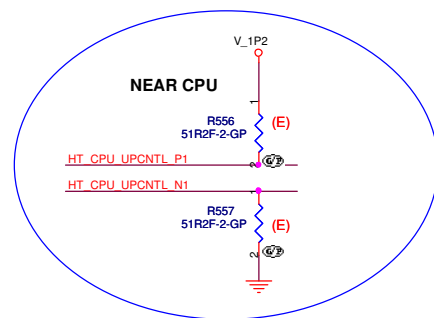
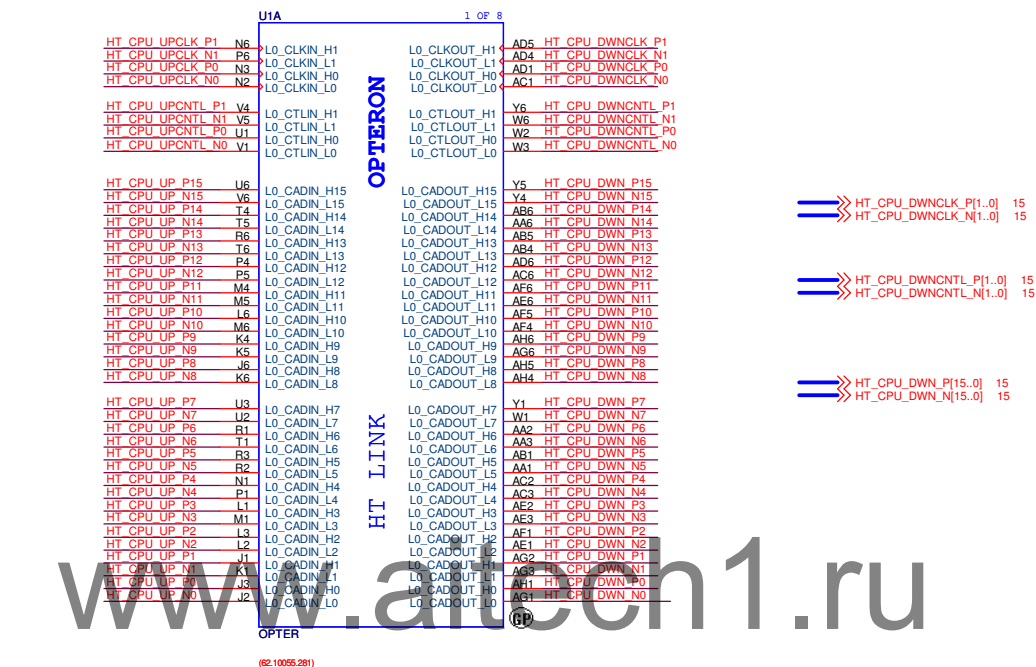
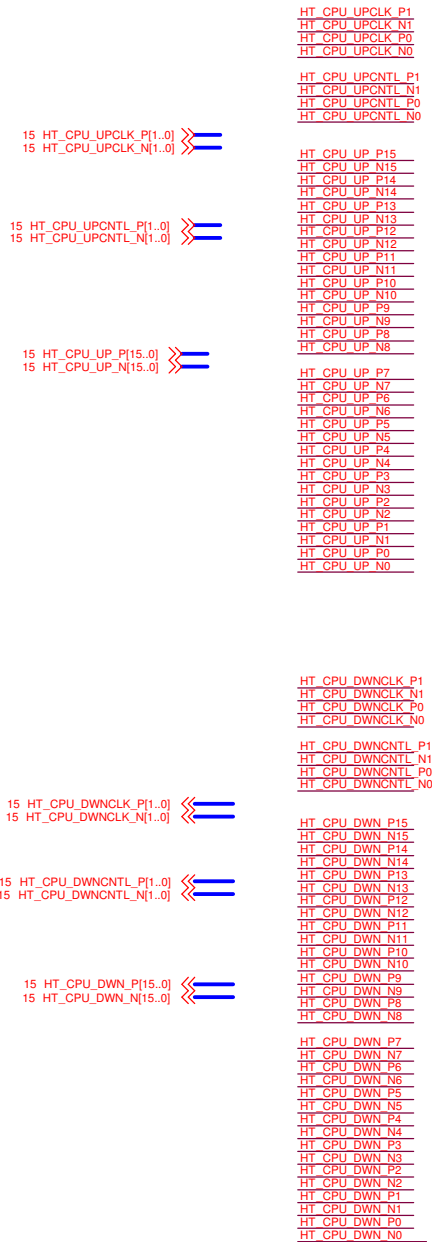
G:For GIGA LAN
M:For 10/100 LAN

U:EuP
N:Non-EuP

<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title GPIO TABLE			
Size A3	Document Number eMaguire	Rev 1M	
Date:	Thursday, February 11, 2010	Sheet	6 of 46

HT BUS



E for MCP61 05/07

B for MCP78 05/07

NEAR CPU

<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title CPU HT INTERFACE			
Size A3	Document Number eMaguire	Rev 1M	
Date:	Thursday, February 11, 2010	Sheet	7 of 46

5 CPU_CLK_P >> CPU_CLK_P
5 CPU_CLK_N >> CPU_CLK_N

15	CPU_CLK_P	>>>	CPU_CLK_P
15	CPU_CLK_N	>>>	CPU_CLK_N
15,40	HT_CPU_PWRGD	>>>	HT_CPU_PWRGD
15	HT_CPU_STOP*	>>>	HT_CPU_STOP*
15	HT_CPU_RST*	>>>	HT_CPU_RST*

```
15 CPU_THERM_ALERT* << CPU_THERM_ALERT*

40 CPU_CORE_FB << CPU_CORE_FB
40 CPU_CORE_FB* << CPU_CORE_FB*
```

CPU_VID1/SEL >> CPU_VID1/SEL 40

CPU_VID5	CPU_VID5	40
CPU_VID4	CPU_VID4	40
CPU_VID3/SVC	CPU_VID3/SVC	40
CPU_VID2/SVC	CPU_VID2/SVC	40
CPU_VID1/SEL	CPU_VID1/SEL	40
CPU_VID0	CPU_VID0	40

```

CPU_THERMDC CPU_THERMDC 31
CPU_THERMDA CPU_THERMDA 31
CPU_THERMTSRP:

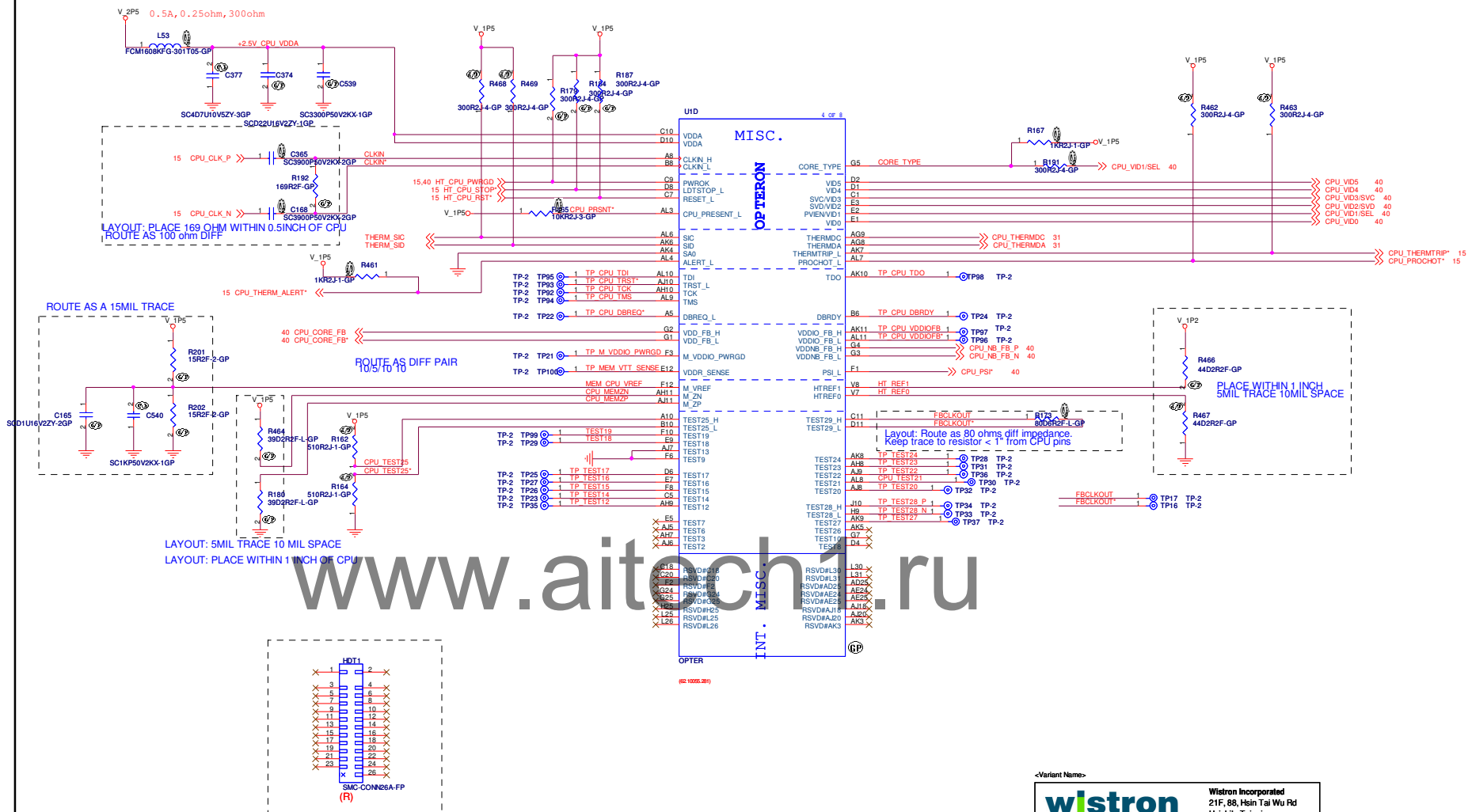
```

```


CPU_PROCHOT* 15
CPU_NB_FB_P 40
CPU_NB_FB_N 40

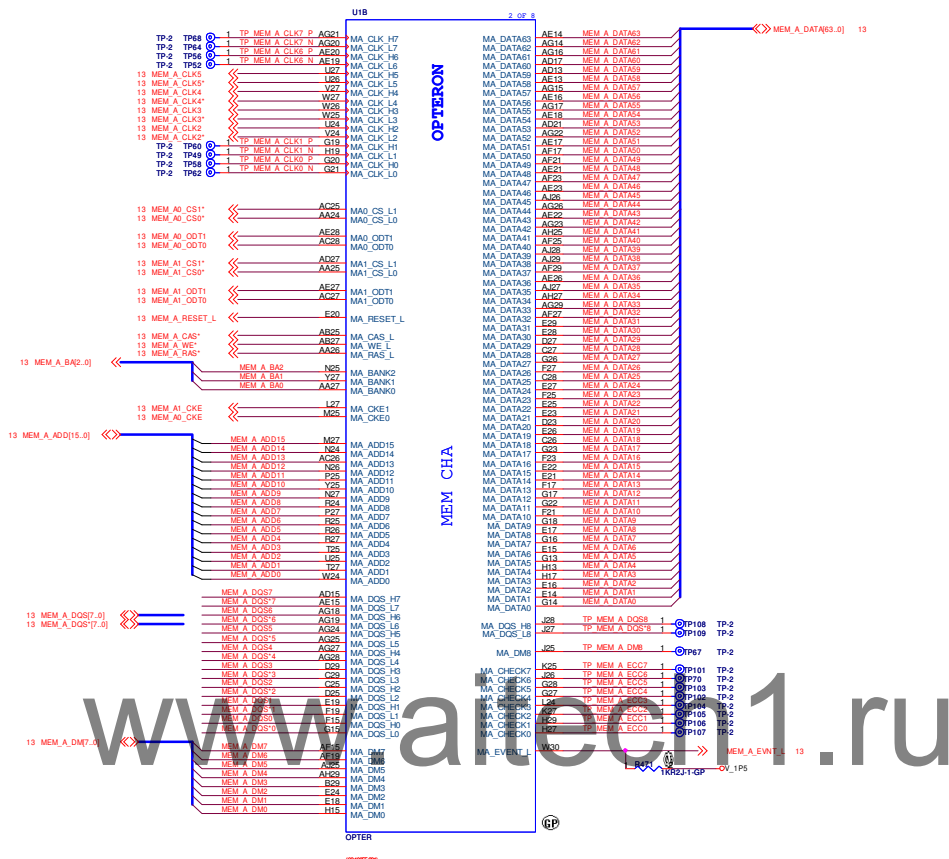
```

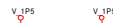
CPU PSF >> CPU PSr 40

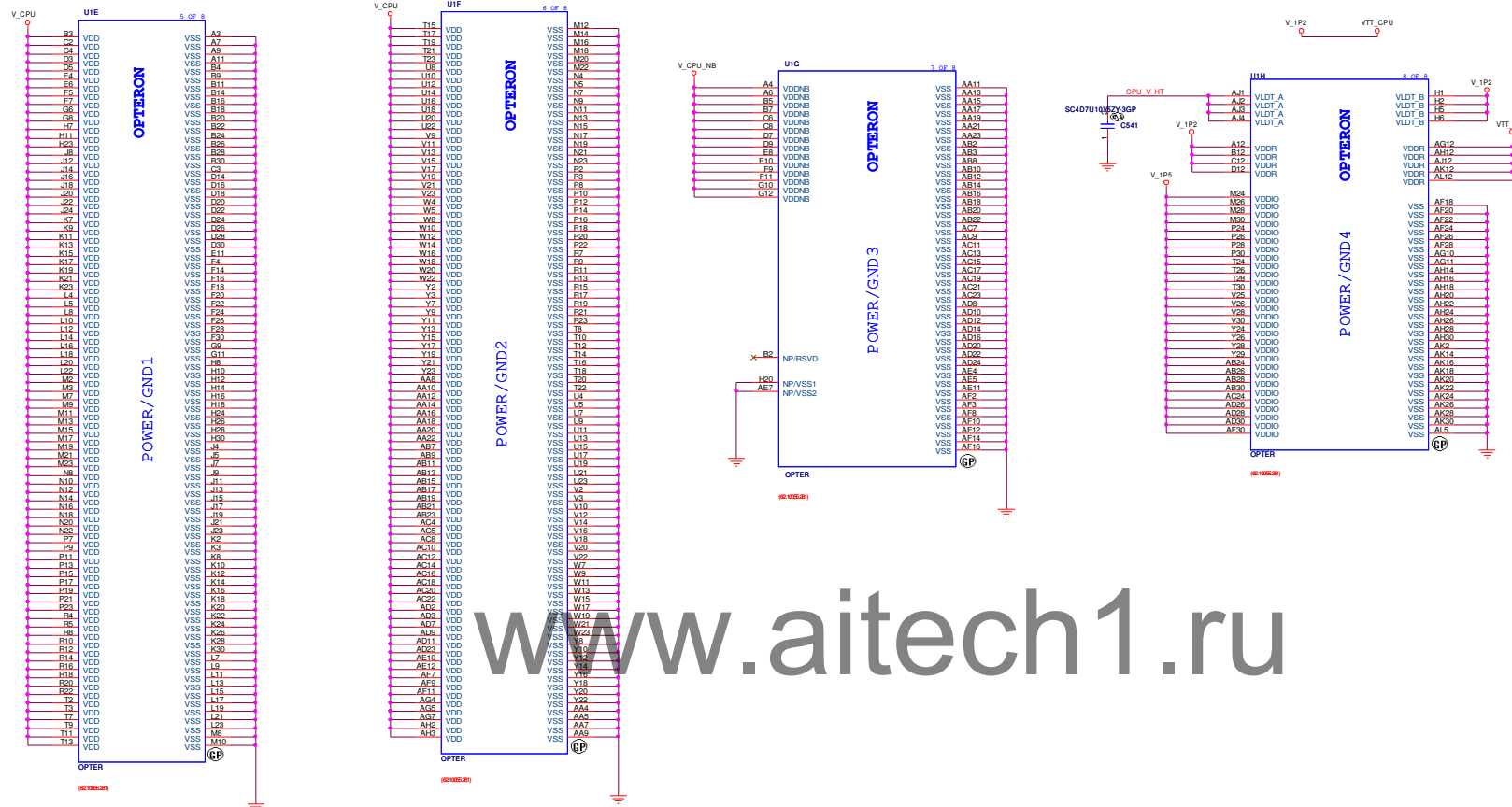


<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title CPU CNTL/STRAPS			
Size	Document Number		Rev
	CustomMaguire		1
Date	Thursday	February 11 2010	Rheet R of 4R

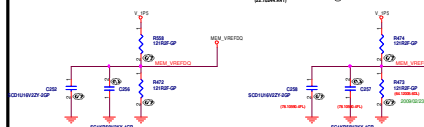
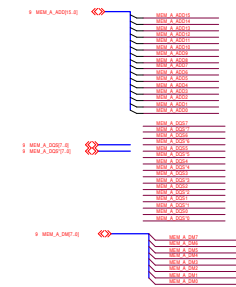
[illegible]

[illegible]



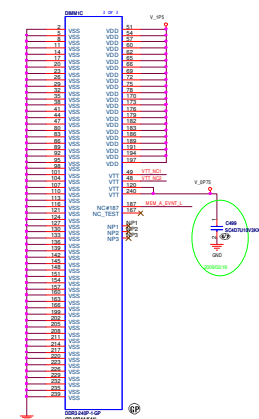
DIMM 1

DIMM 1



Closest DIMM to CPU
Channel "A" Lower 64 bits

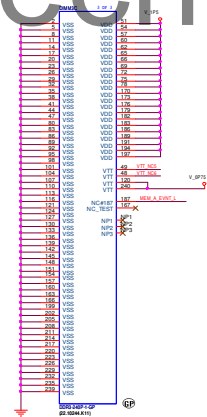
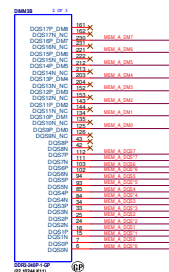
Closest DIMM to CPU
Channel "A" Lower 64 bits



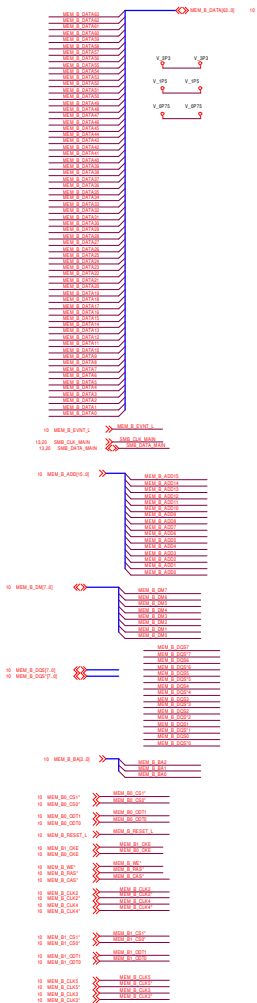
DIMM 3

CHANNEL "A" LOWER 64 BITS

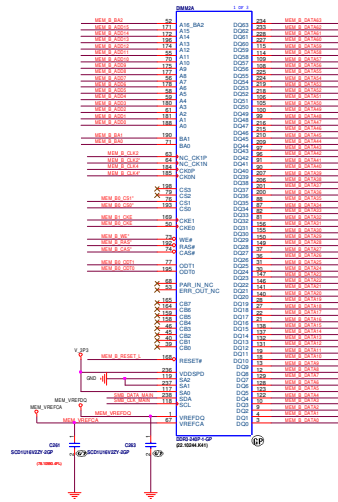
CHANNEL "A" LOWER 64 BITS



Memory CHB

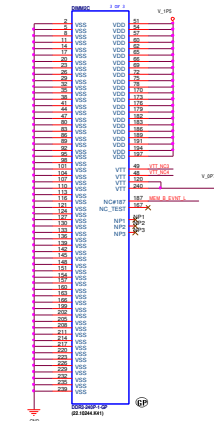
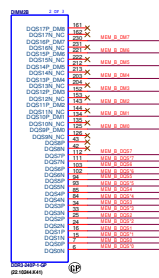


DIMM 2

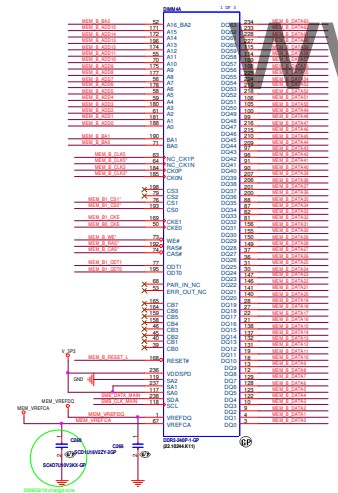


DATA	DATA	DATA
DQ00	DQ01	DQ02
DQ03	DQ04	DQ05
DQ06	DQ07	DQ08
DQ09	DQ10	DQ11
DQ12	DQ13	DQ14
DQ15	DQ16	DQ17
DQ18	DQ19	DQ20
DQ21	DQ22	DQ23
DQ24	DQ25	DQ26
DQ27	DQ28	DQ29
DQ30	DQ31	DQ32
DQ33	DQ34	DQ35
DQ36	DQ37	DQ38
DQ39	DQ40	DQ41
DQ42	DQ43	DQ44
DQ45	DQ46	DQ47
DQ48	DQ49	DQ50
DQ51	DQ52	DQ53
DQ54	DQ55	DQ56
DQ57	DQ58	DQ59
DQ60	DQ61	DQ62
DQ63	DQ64	DQ65
DQ66	DQ67	DQ68
DQ69	DQ70	DQ71
DQ72	DQ73	DQ74
DQ75	DQ76	DQ77
DQ78	DQ79	DQ80
DQ81	DQ82	DQ83
DQ84	DQ85	DQ86
DQ87	DQ88	DQ89
DQ90	DQ91	DQ92
DQ93	DQ94	DQ95
DQ96	DQ97	DQ98
DQ99	DQ100	DQ101

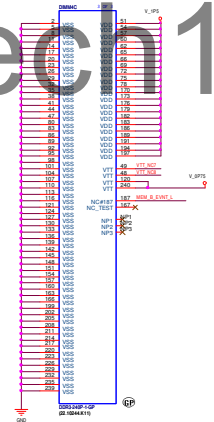
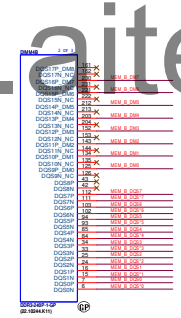
CHANNEL 0: UPPER BANKS



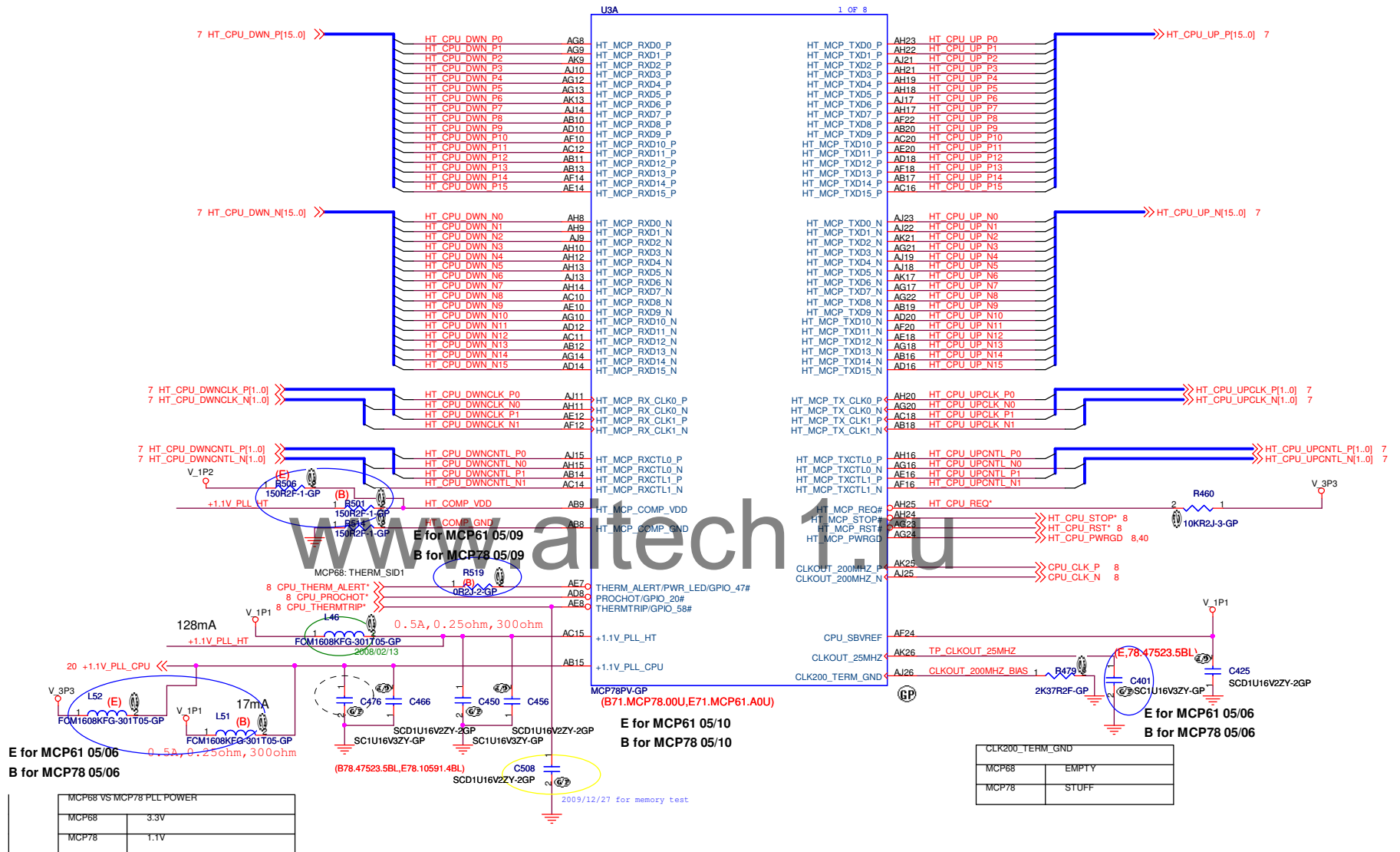
DIMM 4



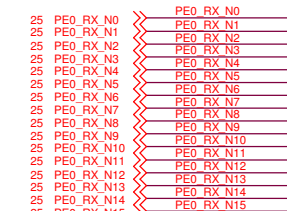
DATA	DATA	DATA
DQ00	DQ01	DQ02
DQ03	DQ04	DQ05
DQ06	DQ07	DQ08
DQ09	DQ10	DQ11
DQ12	DQ13	DQ14
DQ15	DQ16	DQ17
DQ18	DQ19	DQ20
DQ21	DQ22	DQ23
DQ24	DQ25	DQ26
DQ27	DQ28	DQ29
DQ30	DQ31	DQ32
DQ33	DQ34	DQ35
DQ36	DQ37	DQ38
DQ39	DQ40	DQ41
DQ42	DQ43	DQ44
DQ45	DQ46	DQ47
DQ48	DQ49	DQ50
DQ51	DQ52	DQ53
DQ54	DQ55	DQ56
DQ57	DQ58	DQ59
DQ60	DQ61	DQ62
DQ63	DQ64	DQ65
DQ66	DQ67	DQ68
DQ69	DQ70	DQ71
DQ72	DQ73	DQ74
DQ75	DQ76	DQ77
DQ78	DQ79	DQ80
DQ81	DQ82	DQ83
DQ84	DQ85	DQ86
DQ87	DQ88	DQ89
DQ90	DQ91	DQ92
DQ93	DQ94	DQ95
DQ96	DQ97	DQ98
DQ99	DQ100	DQ101



HT_CPU_DWN_P[15..0] >>>>
7 HT_CPU_DWN_N[15..0] >>>>
7 HT_CPU_DWNCNK_P[1..0] >>>>
7 HT_CPU_DWNCNK_N[1..0] >>>>
HT_CPU_DWNCNTL_P[1..0] >>>>
HT_CPU_DWNCNTL_N[1..0] >>>>
8 CPU_THERM_ALERT* >>>>
8 CPU_PROCHOT* >>>>
8 CPU_THERMTRIP* >>>>
20 +1.1V_PL1_CPU <<<<
7 HT_CPU_UP_P[15..0] <<<<
7 HT_CPU_UP_N[15..0] <<<<
7 HT_CPU_UPCLK_P[1..0] <<<<
7 HT_CPU_UPCLK_N[1..0] <<<<
HT_CPU_UPCNTL_P[1..0] <<<<
HT_CPU_UPCNTL_N[1..0] <<<<
8 HT_CPU_STOP* <<<<
8 HT_CPU_RST* <<<<
8,40 HT_CPU_PWRGD <<<<



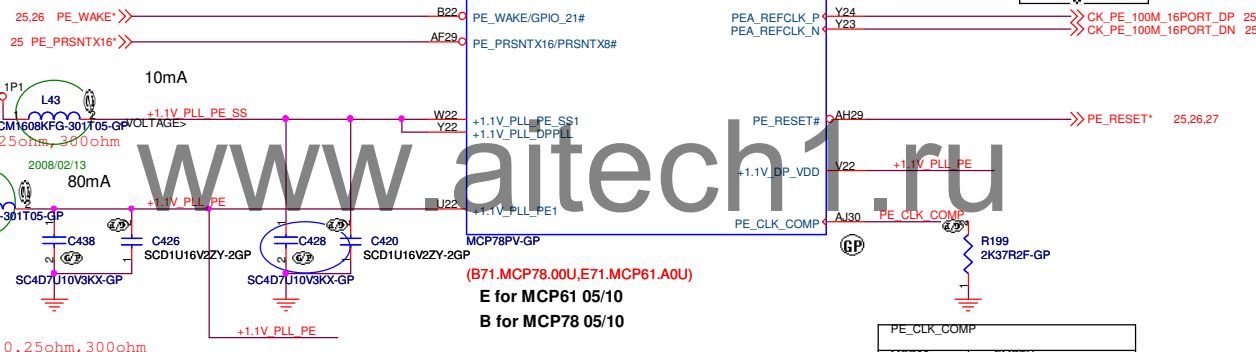
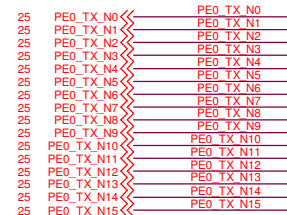
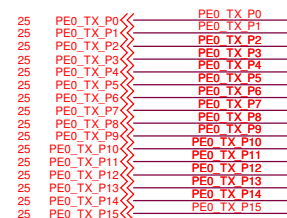
PE0_RX_P0	PE0_RX_P0
PE0_RX_P1	PE0_RX_P1
PE0_RX_P2	PE0_RX_P2
PE0_RX_P3	PE0_RX_P3
PE0_RX_P4	PE0_RX_P4
PE0_RX_P5	PE0_RX_P5
PE0_RX_P6	PE0_RX_P6
PE0_RX_P7	PE0_RX_P7
PE0_RX_P8	PE0_RX_P8
PE0_RX_P9	PE0_RX_P9
PE0_RX_P10	PE0_RX_P10
PE0_RX_P11	PE0_RX_P11
PE0_RX_P12	PE0_RX_P12
PE0_RX_P13	PE0_RX_P13
PE0_RX_P14	PE0_RX_P14
PE0_RX_P15	PE0_RX_P15



25,26 PE_WAKE* >>> _____

25 PE PRSNTX16* >>> _____

25 CK_PE_100M_16PORT_DP <<—
25 CK_PE_100M_16PORT_DN <<—
25,26,27 PE RESET* <<—



PE_CLK_COMP	
MCP68	EMPTY
MCP78	STUFF

<Variant Name>



Wlstron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

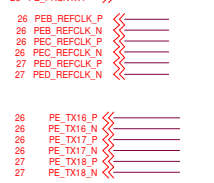
Title *MCP61 PEX X16*

Size A3	Document Number eMaguire	Rev 1M
Date:	Thursday, February 11, 2010	Sheet 16 of 46

26 PE_RX16_P
26 PE_RX16_N
26 PE_RX17_P
26 PE_RX17_N
27 PE_RX18_P
27 PE_RX18_N

26 PEA_PRSN1*
26 PEB_PRSN1*
25 PE_PRSN1X1*

25 PE_PRSN1X8* PE_PRSN1X8*
25 PE_PRSN1X4* PE_PRSN1X4*



```

30  RGMII_RXD[3..0]  >>>
30  RGMII_RXC
30  RGMII_RXCTL  >>>
30  ENREG/RXER_N
30  COL_N
30  CRS_N
30  RGMII_INTR*  >>>
30  RGMII_TXC
30  RGMII_TXCTL
30  RGMII_MDC
30  RGMII_MDIO
30  RGMII_25MHz
30  RGMII_RESET

```

24 RGB_DAC_RED <<< _____
24 RGB_DAC_GREEN <<< _____
24 RGB_DAC_BLUE <<< _____

24 RGB_DAC_HSYNC <<< _____
24 RGB_DAC_VSYNC <<< _____

24 RGB_DDC_SCL <<< _____
24 RGB_DDC_SDA <<< _____

```

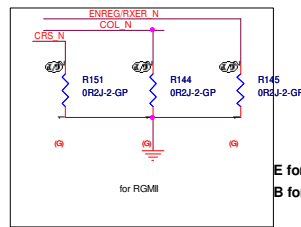
23 HDMI_DVI_SCL <<=====
23 HDMI_DVI_SDA <<=====

23 HDMI_DVI_TXD0P <<=====
23 HDMI_DVI_TXD0N <<=====
23 HDMI_DVI_TXD1P <<=====
23 HDMI_DVI_TXD1N <<=====
23 HDMI_DVI_TXD2P <<=====
23 HDMI_DVI_TXD2N <<=====

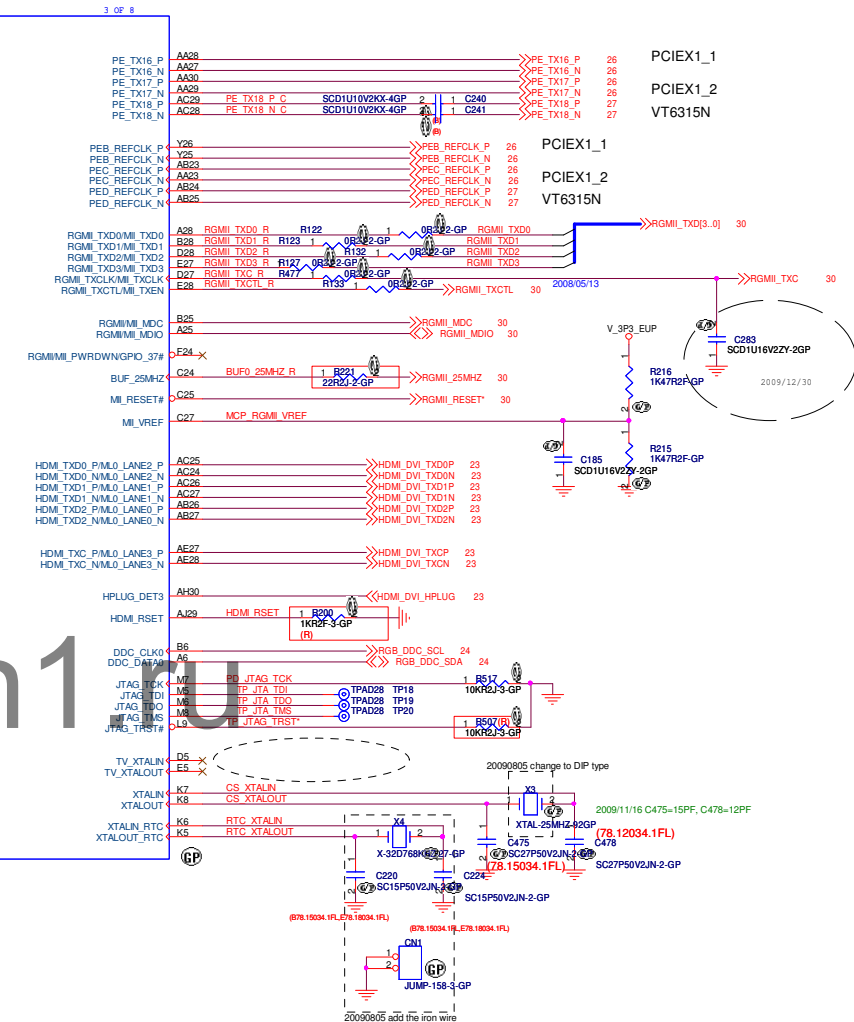
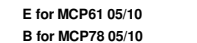
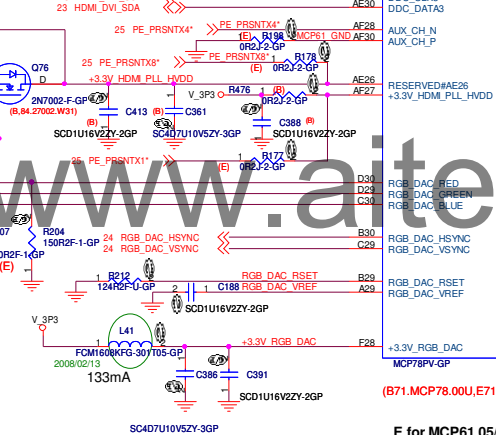
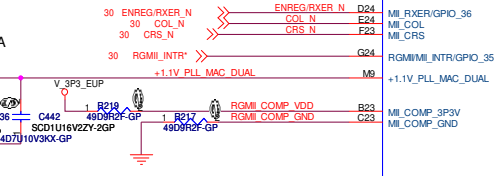
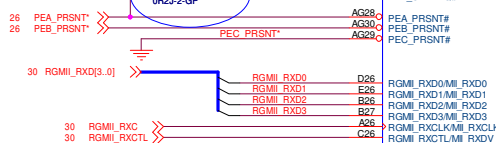
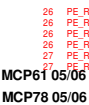
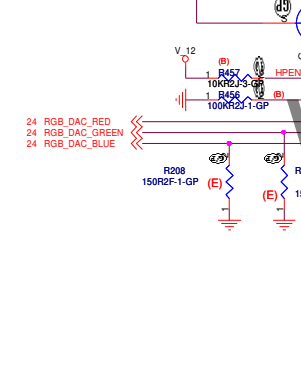
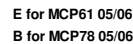
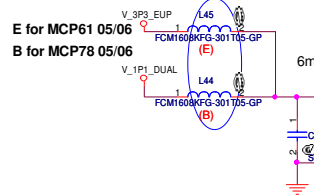
23 HDMI_DVI_TXCP <<=====
23 HDMI_DVI_TXCN <<=====

23 HDMI_DVI_HPLUG >>=====

```



MCP68 VS MCP78 PLL POWER	
MCP68	3.3V
MCP78	1.1V



<Variant Name>

LPC

31 LPC_AD0 <<> LPC_AD0
31 LPC_AD1 <<> LPC_AD1
31 LPC_AD2 <<> LPC_AD2
31 LPC_AD3 <<> LPC_AD3

22,31 LPC_FRAME* <<>

31 LPC_SERIRQ <<>

31 LPC_CLK_SIO <<>

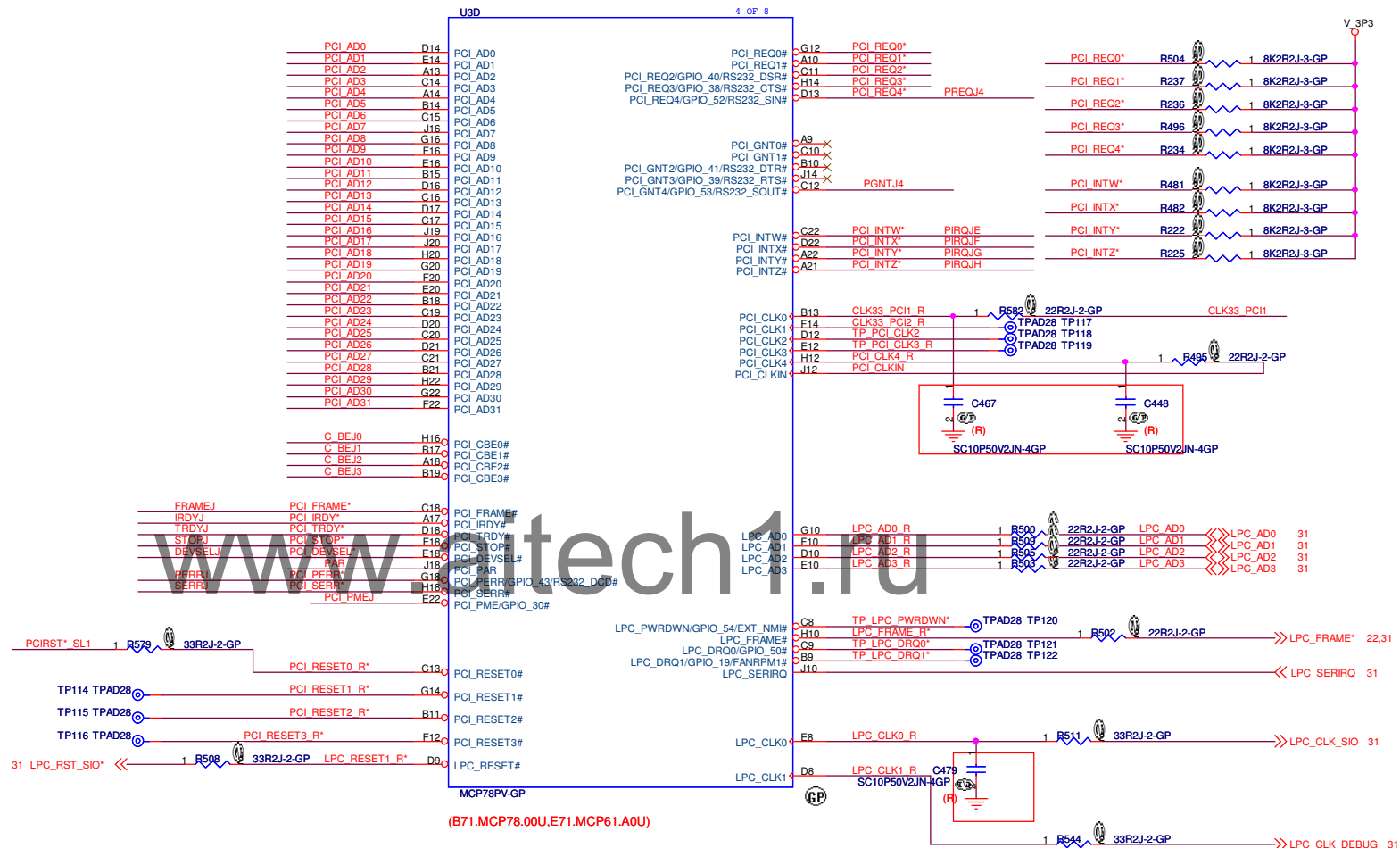
31 LPC_CLK_DEBUG <<>

31 LPC_RST_SIO* <<>

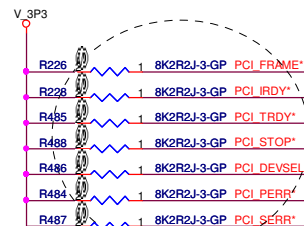
PCI

46 PCI_AD0 <<> PCI_AD0
46 PCI_AD1 <<> PCI_AD1
46 PCI_AD2 <<> PCI_AD2
46 PCI_AD3 <<> PCI_AD3
46 PCI_AD4 <<> PCI_AD4
46 PCI_AD5 <<> PCI_AD5
46 PCI_AD6 <<> PCI_AD6
46 PCI_AD7 <<> PCI_AD7
46 PCI_AD8 <<> PCI_AD8
46 PCI_AD9 <<> PCI_AD9
46 PCI_AD10 <<> PCI_AD10
46 PCI_AD11 <<> PCI_AD11
46 PCI_AD12 <<> PCI_AD12
46 PCI_AD13 <<> PCI_AD13
46 PCI_AD14 <<> PCI_AD14
46 PCI_AD15 <<> PCI_AD15
46 PCI_AD16 <<> PCI_AD16
46 PCI_AD17 <<> PCI_AD17
46 PCI_AD18 <<> PCI_AD18
46 PCI_AD19 <<> PCI_AD19
46 PCI_AD20 <<> PCI_AD20
46 PCI_AD21 <<> PCI_AD21
46 PCI_AD22 <<> PCI_AD22
46 PCI_AD23 <<> PCI_AD23
46 PCI_AD24 <<> PCI_AD24
46 PCI_AD25 <<> PCI_AD25
46 PCI_AD26 <<> PCI_AD26
46 PCI_AD27 <<> PCI_AD27
46 PCI_AD28 <<> PCI_AD28
46 PCI_AD29 <<> PCI_AD29
46 PCI_AD30 <<> PCI_AD30
46 PCI_AD31 <<> PCI_AD31
46 PCI_CBE#0 <<> C_BEJ0
46 PCI_CBE#1 <<> C_BEJ1
46 PCI_CBE#2 <<> C_BEJ2
46 PCI_CBE#3 <<> C_BEJ3
46 PCI_FRAME# <<> FRAMEJ
46 PCI_DEVSEL# <<> DEVSELJ
46 PCI_IRDY# <<> IRDYJ
46 PCI_TRDY# <<> TRDYJ
46 PCI_PAR <<> PAR
46 PCI_STOP# <<> STOPJ
46 PCI_PERR# <<> PERRJ
46 PCI_SERR# <<> SERRJ

46 PCI_REQ#4 <<> PREQJ4
46 PCI_GNT#4 <<> PGNTJ4
46 PCI_INT#4 <<> PIRQJE
46 PCI_INT#5 <<> PIRQJF
46 PCI_INT#6 <<> PIRQJG
46 PCI_INT#7 <<> PIRQJH
46 PCI_INT#8 <<> CLK33_PCH1
46 CLK33_PCH1 <<>
46 PCIRST1# <<> PCIRST* SL1
46 PCIRST1# <<>
46 PCIPME# <<> PCIPMEJ



(B71.MCP78.00U,E71.MCP61.A0U)
E for MCP61 05/10
B for MCP78 05/10



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
MCP61 PCI/LPC

Size
A3
Document Number
eMagure

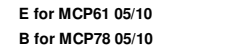
Rev
1M


Date: Thursday, February 11, 2010 Sheet 18 of 46

28 SATA_C1_TX_C_P <<—
28 SATA_C1_TX_C_N <<—

28 SATA_C1_RX_C_N <<—
28 SATA_C1_RX_C_P <<—

35 ICH_SATA_LED* <<—



		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title <i>MCP61 SATA/IDE</i>			
Size	Document Number	Rev	
	Customer Magazine	1M	
Date:	Thursday, February 11, 2010	Sheet	19 of 46


```

37 HDA_BITCLK
37,38 HDA_RST*
37 HDA_SYNC
22,37 HDA_SDOUT
37 HDA_SDIN_0
37 FP_AUDIO_PRESENCE*

```

```

22  SPI_DI      >>>_____
22  SPI_DO      >>>_____
22  SPI_CS*     >>>_____
22  SPI_CLK     >>>_____

```

```
31 DEBUG_INTR    <<—
15 +1.1V_PLL_CPU >>—
```

35 RTC_RST* >>> _____

43 MEM_VLD >>> _____

44 HT_VLD >>> _____

42,44 HTVDD_EN >>> _____

40 CPU_VLD >>> _____

40 CPUVDD_EN <<< _____

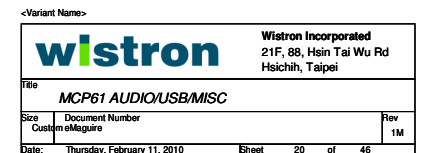
35	FP_RESET*	↗
31,34,43,45	SLP_S5*	↗
31,35,39	SLP_S3*	↗
34,45	PWRGD_SB	↗
34	PS_PWRGD	↗

13,14 SMB_CLK_MAIN <<—
13,14 SMB_DATA_MAIN <<—
5,26,46 SMB_CLK_RESUME <<—
5,46 SMB_DATA_RESUME <<—

```

31,37 SPEAKER
31,45 SB_PWRON*
31 SIO_PME*
31 SIO_KBRST*
31 A20GATE
28 USB_OC_01*
29 USB_OC_23*
29 USB_OC_45*
29 USB_OC_67*

```

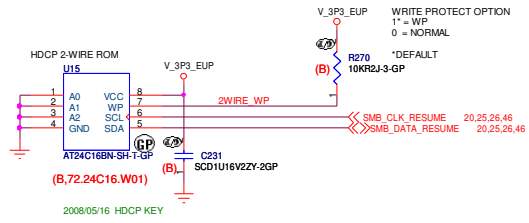


22 +1.1V_HT_A <<—————

22 +1.1V_PEX_A <<—————

22 +1.1V_SP_A <<—————

20,25,26,46 SMB_CLK_RESUME >>>
20,25,26,46 SMB_DATA_RESUME <<<



E for MCP61 05/10
B for MCP78 05/10

Power

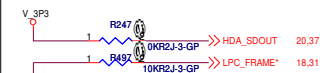
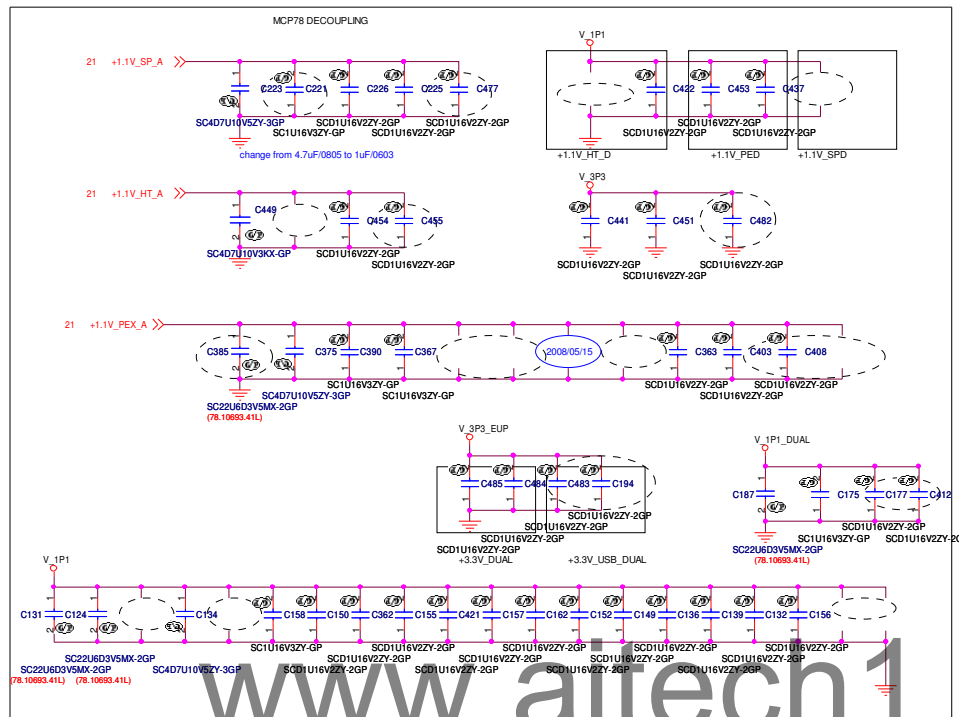
21 +1.1V_SP_A >>
21 +1.1V_HT_A >>
21 +1.1V_PEX_A >>

SPI

20 SPI_CS* >>
20 SPI_DI >>
31 SPI_WP* >>
20 SPI_CLK >>
20 SPI_DO >>

HDA

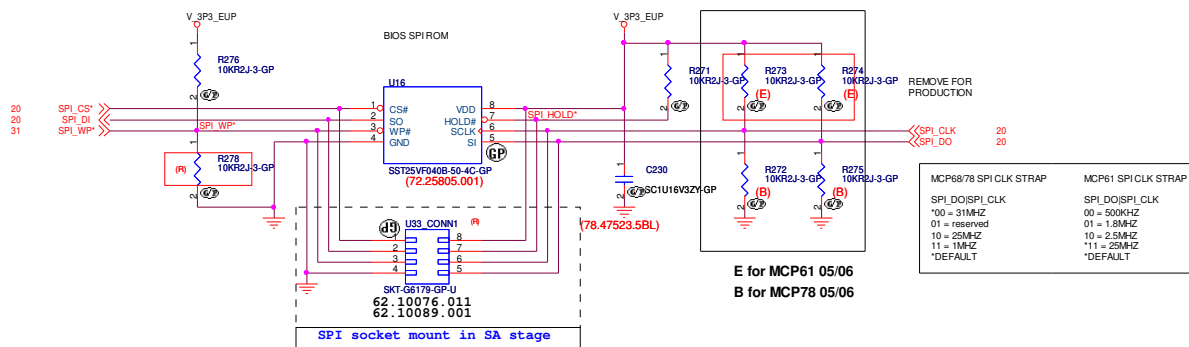
20,37 HDA_SDOUT <<
18,31 LPC_FRAME* <<



BIOS FLASH SELECT

STRAP	HDA_SDOUT	LPC_FRAME*
LPC BIOS	0	0
PCI BIOS	0	1
SPI BIOS	1 *	0 *
RESERVED	1	1

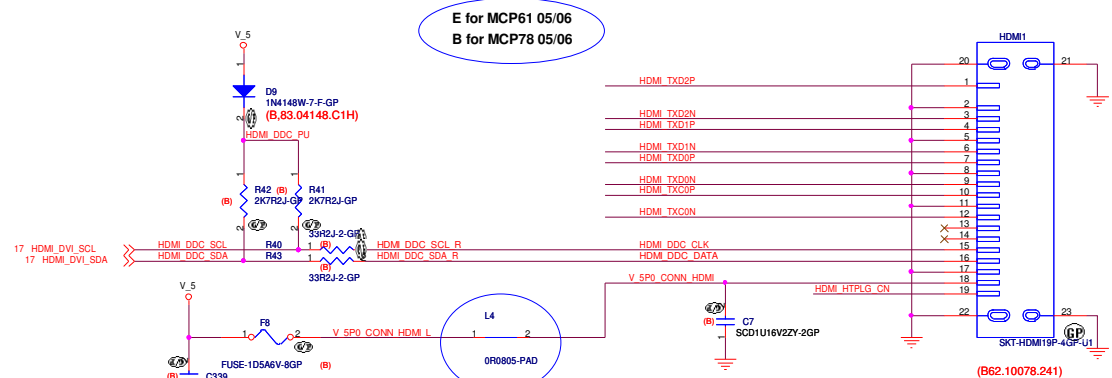
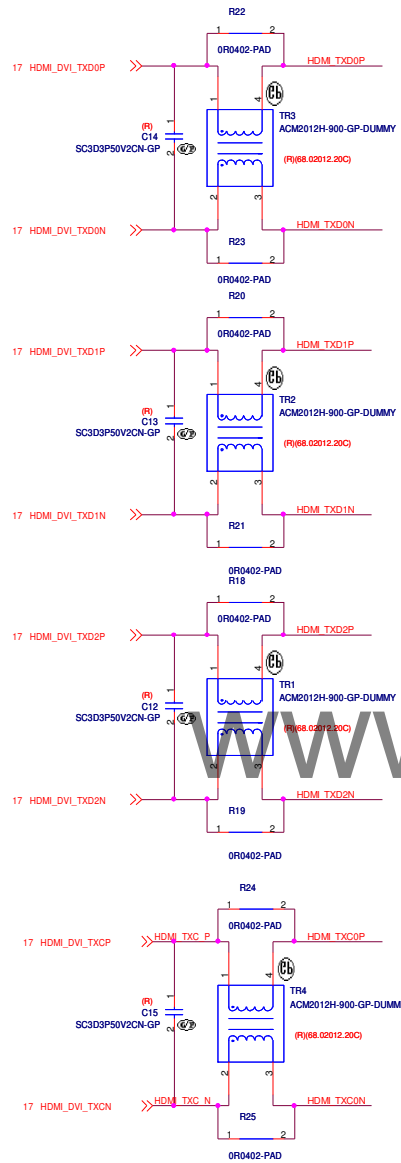
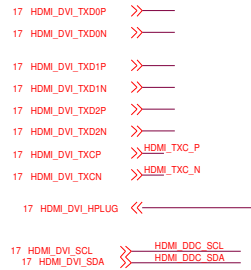
*DEFAULT



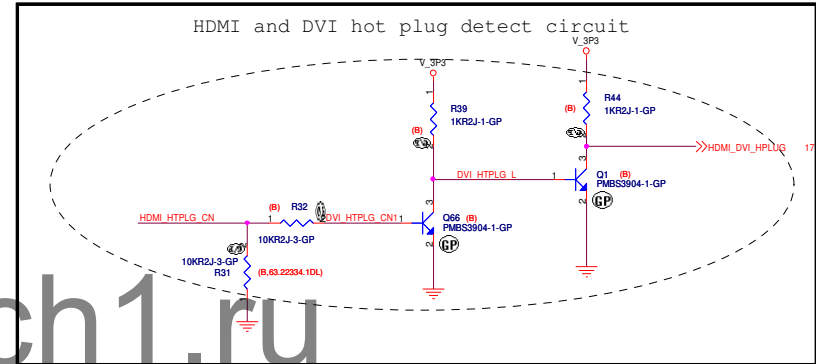
<Variant Name>

wlstron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title MCP61 DECOUPLING/SPI			
Size Custom	Document Number eMaguire		Rev 1M
Date:	Thursday, February 11, 2010	Sheet	22 of 46

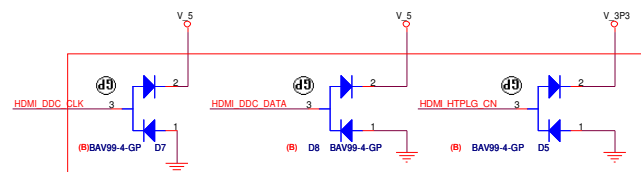
HDMI



E for MCP61 05/06
B for MCP78 05/06



CLOSED TO HDMI CONNECTOR

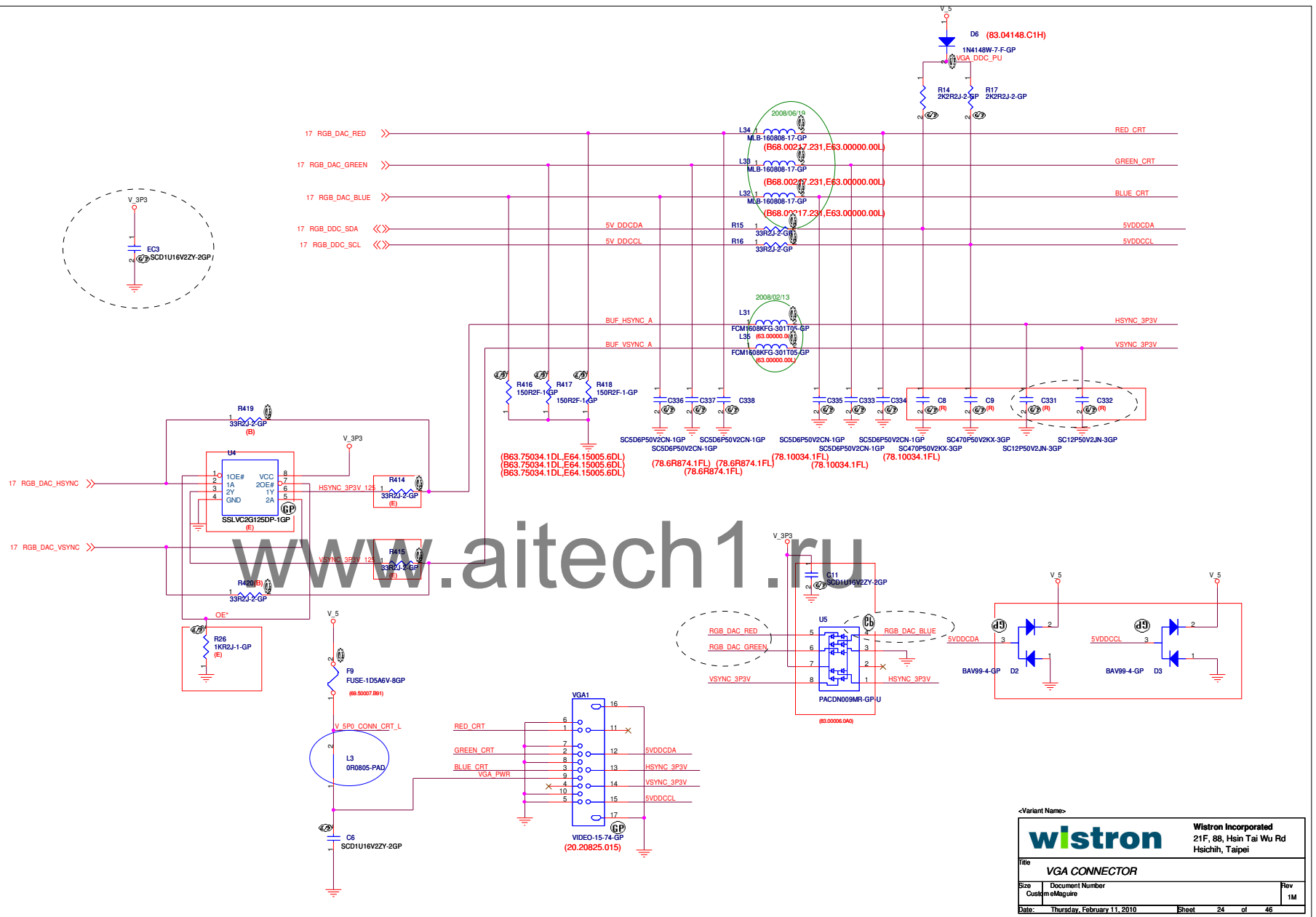



<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
File HDMI CONNECTOR			
Size	Document Number	Rev	
Cust	Signature	1M	
Date:	Thursday, February 11, 2010	Sheet	23 of 46

VGA

- 17 RGB_DAC_RED >>
- 17 RGB_DAC_GREEN >>
- 17 RGB_DAC_BLUE >>
- 17 RGB_DDC_SDA << 5V DDCDA
- 17 RGB_DDC_SCL << 5V DDCCL
- 17 RGB_DAC_HSYNC >>
- 17 RGB_DAC_VSYNC >>



<Variant Name>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
			
file		VGA CONNECTOR	
Size	Document Number	Rev	
	Custom enligature	1M	
Date:	Thursday, February 11, 2010	Sheet	24 of 46

PCIEX16

20,21,26,46 SMB_CLK_RESUME
20,21,26,46 SMB_DATA_RESUME

16,26 PE_WAKE* <<
16 PE0_TX_P15 >>
16 PE0_TX_N15 >>
17 PE_PRSTNTX1* <<
16 PE0_TX_P14 >>
16 PE0_TX_N14 >>
16 PE0_TX_P13 >>
16 PE0_TX_N13 >>
16 PE0_TX_P12 >>
16 PE0_TX_N12 >>
17 PE_PRSTNTX4* <<
16 PE0_TX_P11 >>
16 PE0_TX_N11 >>
16 PE0_TX_P10 >>
16 PE0_TX_N10 >>
16 PE0_TX_P9 >>
16 PE0_TX_N9 >>
16 PE0_TX_P8 >>
16 PE0_TX_N8 >>
17 PE_PRSTNTX8* <<
16 PE0_TX_P7 >>
16 PE0_TX_N7 >>
16 PE0_TX_P6 >>
16 PE0_TX_N6 >>
16 PE0_TX_P5 >>
16 PE0_TX_N5 >>
16 PE0_TX_P4 >>
16 PE0_TX_N4 >>
16 PE0_TX_P3 >>
16 PE0_TX_N3 >>
16 PE0_TX_P2 >>
16 PE0_TX_N2 >>
16 PE0_TX_P1 >>
16 PE0_TX_N1 >>
16 PE0_TX_P0 >>
16 PE0_TX_N0 >>
16 PE_PRSTNTX16* <<
16,26,27 PE_RESET* >>

16 CK_PE_100M_16PORT_DP >>
16 CK_PE_100M_16PORT_DN >>

16 PE0_RX_P15 <<
16 PE0_RX_N15 <<
16 PE0_RX_P14 <<
16 PE0_RX_N14 <<
16 PE0_RX_P13 <<
16 PE0_RX_N13 <<
16 PE0_RX_P12 <<
16 PE0_RX_N12 <<
16 PE0_RX_P11 <<
16 PE0_RX_N11 <<
16 PE0_RX_P10 <<
16 PE0_RX_N10 <<
16 PE0_RX_P9 <<
16 PE0_RX_N9 <<
16 PE0_RX_P8 <<
16 PE0_RX_N8 <<
16 PE0_RX_P7 <<
16 PE0_RX_N7 <<
16 PE0_RX_P6 <<
16 PE0_RX_N6 <<
16 PE0_RX_P5 <<
16 PE0_RX_N5 <<
16 PE0_RX_P4 <<
16 PE0_RX_N4 <<
16 PE0_RX_P3 <<
16 PE0_RX_N3 <<
16 PE0_RX_P2 <<
16 PE0_RX_N2 <<
16 PE0_RX_P1 <<
16 PE0_RX_N1 <<
16 PE0_RX_P0 <<
16 PE0_RX_N0 <<

E for MCP61 05/09
B for MCP78 05/09

16 PE_PRSTNTX16* <<

EuP 20090505, change
V_3SB to V_3P3EUP



17 PE_PRSTNTX1* <<

16 PE0_TX_P14 >>
16 PE0_TX_N14 >>

16 PE0_TX_P13 >>
16 PE0_TX_N13 >>

16 PE0_TX_P12 >>
16 PE0_TX_N12 >>

17 PE_PRSTNTX4* <<

16 PE0_TX_P11 >>
16 PE0_TX_N11 >>

16 PE0_TX_P10 >>
16 PE0_TX_N10 >>

16 PE0_TX_P9 >>
16 PE0_TX_N9 >>

16 PE0_TX_P8 >>
16 PE0_TX_N8 >>

17 PE_PRSTNTX8* <<

16 PE0_TX_P7 >>
16 PE0_TX_N7 >>

16 PE0_TX_P6 >>
16 PE0_TX_N6 >>

16 PE0_TX_P5 >>
16 PE0_TX_N5 >>

16 PE0_TX_P4 >>
16 PE0_TX_N4 >>

16 PE0_TX_P3 >>
16 PE0_TX_N3 >>

16 PE0_TX_P2 >>
16 PE0_TX_N2 >>

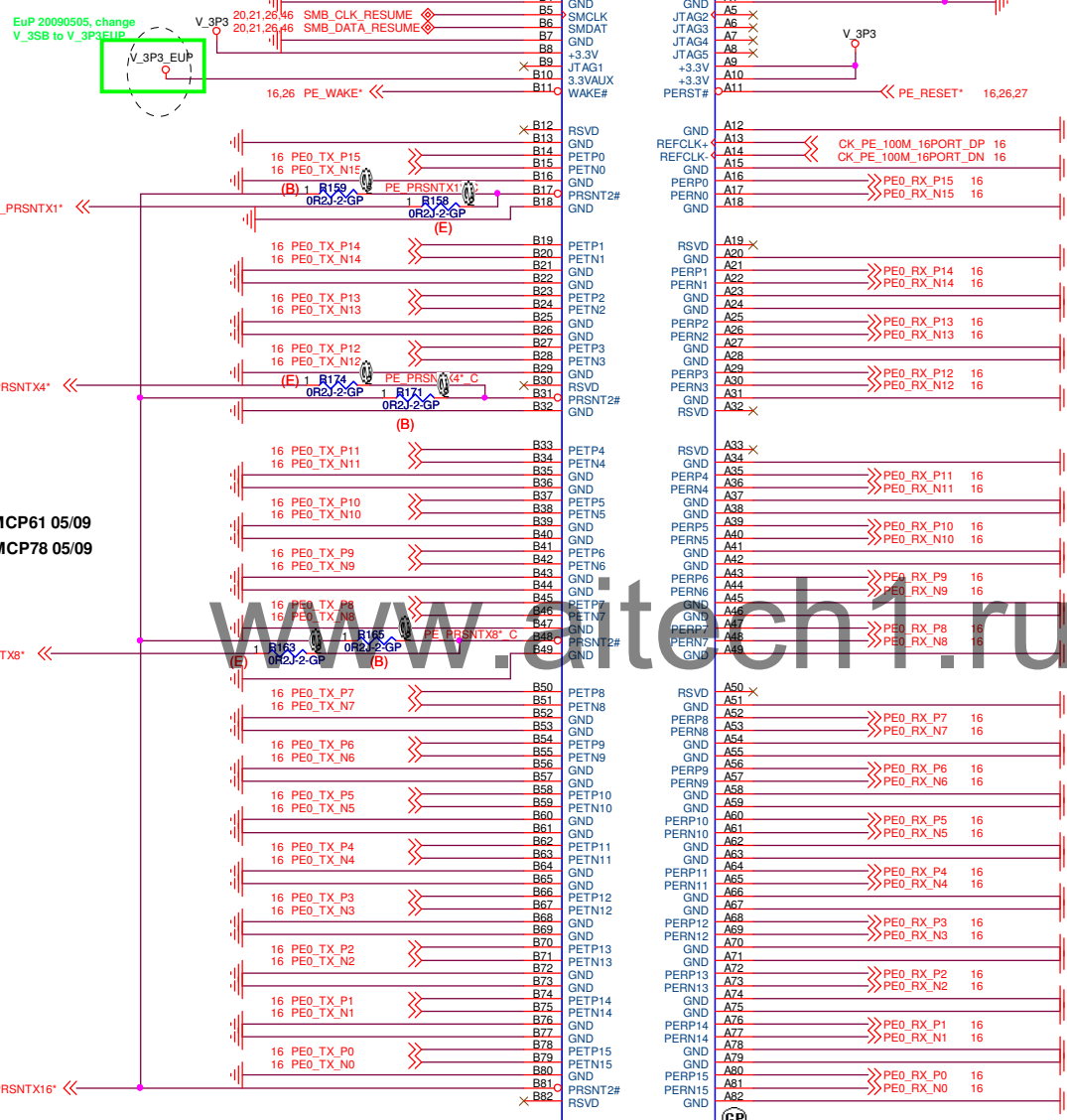
16 PE0_TX_P1 >>
16 PE0_TX_N1 >>

16 PE0_TX_P0 >>
16 PE0_TX_N0 >>

16 PE0_TX_P15 <<
16 PE0_TX_N15 <<

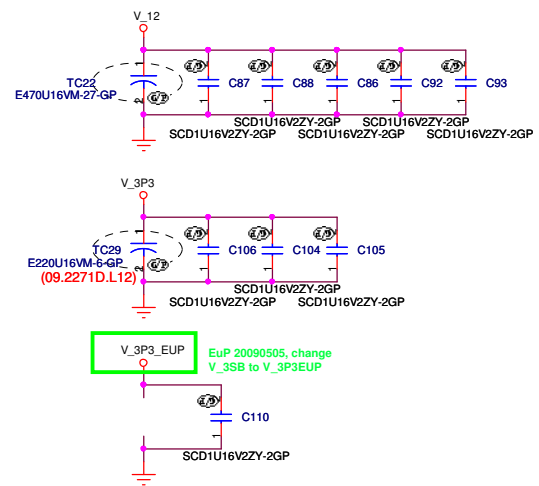
16 PE0_TX_P14 <<
16 PE0_TX_N14 <<

16 PE0_TX_P13 <<
16 PE0_TX_N13 <<



T-CONN164-4R4-GP
(20.50352.164)

2008/01/23



<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title PCIEX16 CONNECTOR			
Size A3	Document Number eMagure		Rev 1M
Date:	Thursday, February 11, 2010	Sheet	25 of 46

PCIEX1

20,21,25,46 SMB_CLK_RESUME >>
20,21,25,46 SMB_DATA_RESUME >>

16,25 PE_WAKE* <<

17 PE_TX16_P >>
17 PE_TX16_N >>
17 PE_TX17_P >>
17 PE_TX17_N >>

17 PEA_PRSTNT* <<
17 PEB_PRSTNT* <<

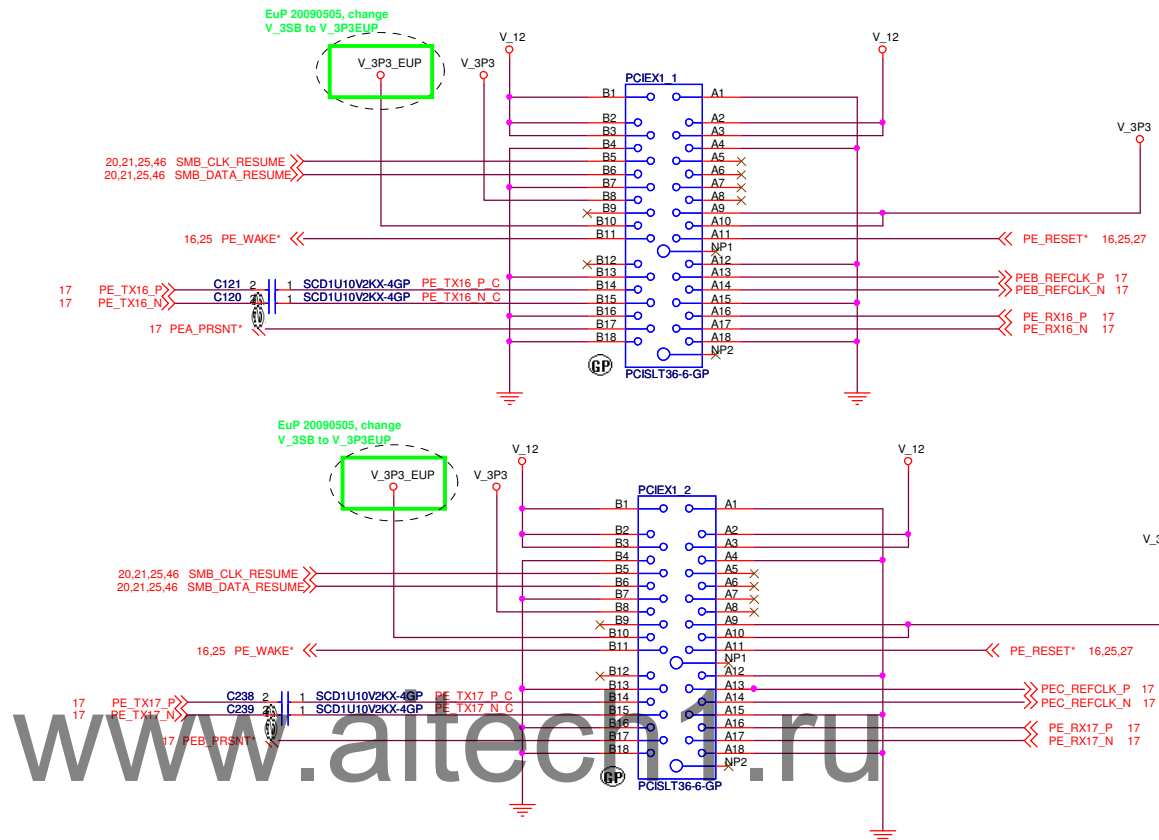
16,25,27 PE_RESET* >>

17 PEB_REFCLK_P <<
17 PEB_REFCLK_N <<

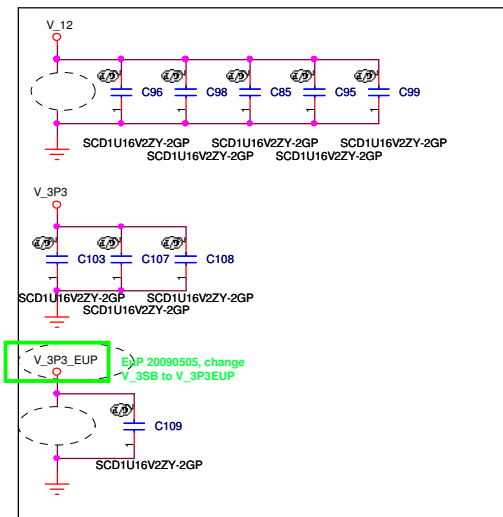
17 PE_RX16_P >>
17 PE_RX16_N >>

17 PEC_REFCLK_P <<
17 PEC_REFCLK_N <<


17 PE_RX17_P >>
17 PE_RX17_N >>



PLACE CAPS NEAR PEX CONNECTORS



<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title PCIEX1 CONNECTOR			
Size A3	Document Number eMaguire		Rev 1M
Date:	Thursday, February 11, 2010	Sheet	26 of 46

PCIEX1

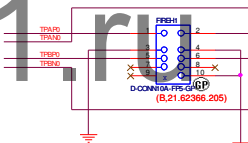
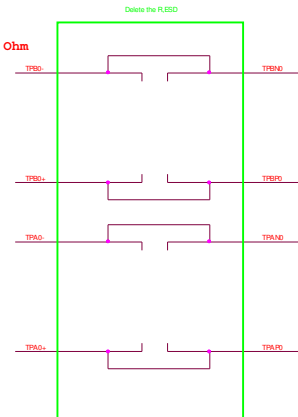
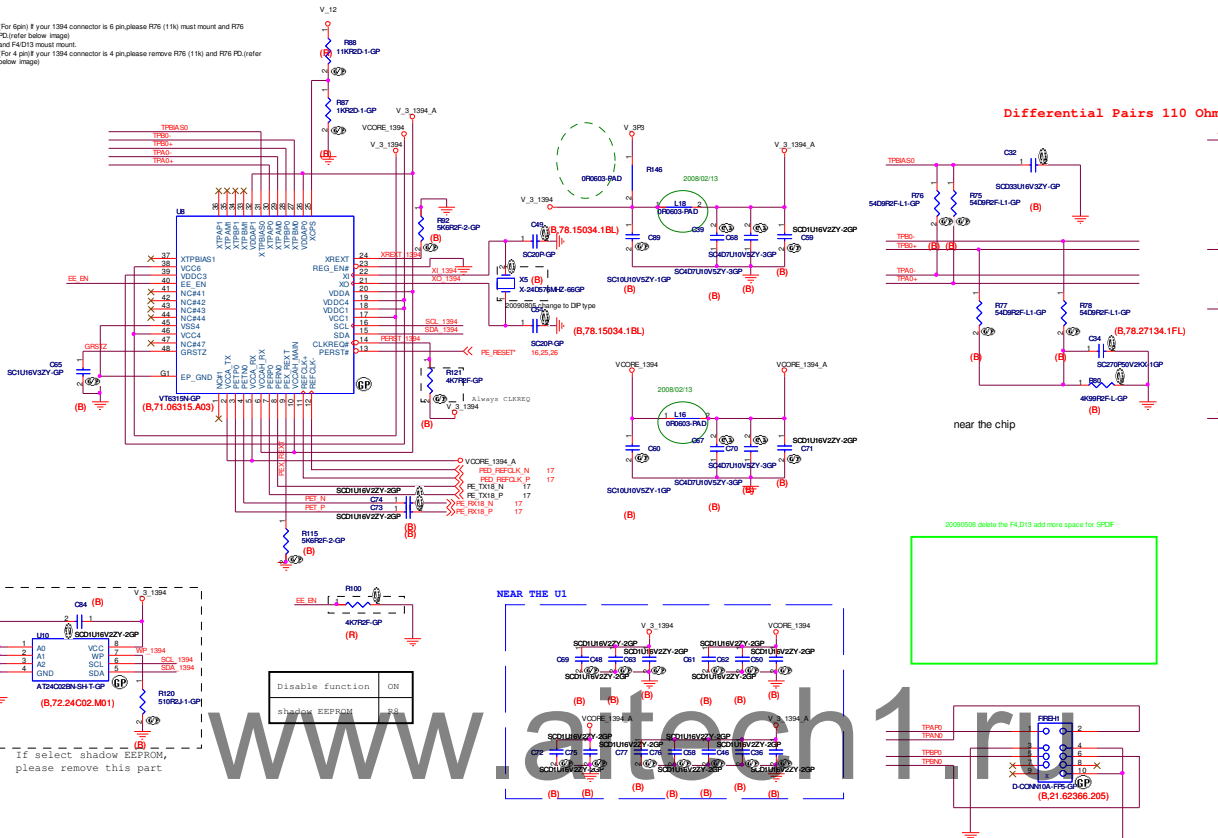
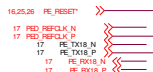
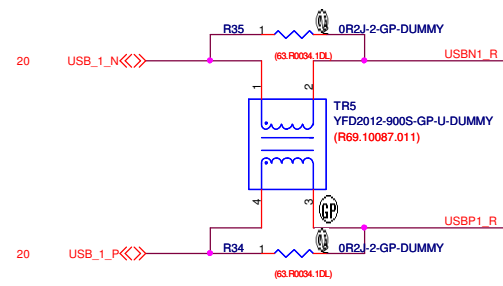
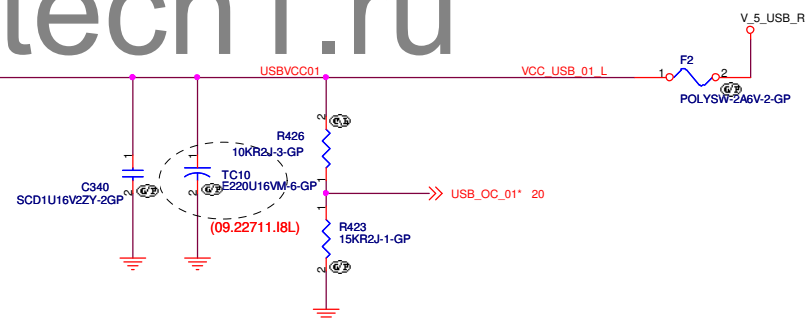
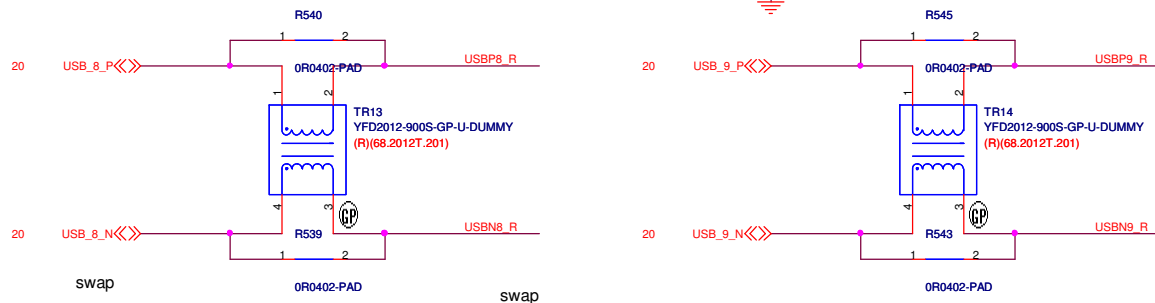


Diagram showing the pin connections for the USB connector:

- Pin 1: USB_8_P
- Pin 2: USB_8_N
- Pin 3: USB_9_P
- Pin 4: USB_9_N
- Pin 5: DATA_C1_RX_C_P
- Pin 6: DATA_C1_RX_C_N
- Pin 7: DATA_C1_TX_C_P
- Pin 8: DATA_C1_TX_C_N




```

20 USB_OC_45 << _____
20 USB_OC_67 << _____
20 USB_OC_23 << _____
20 USB_3_P << _____
20 USB_3_N << _____
20 USB_2_P << _____
20 USB_2_N << _____
20 USB_4_N << _____
20 USB_5_P << _____
20 USB_5_N << _____
20 USB_6_P << _____
20 USB_6_N << _____
20 USB_8_P << _____
20 USB_8_N << _____
20 USB_7_P << _____

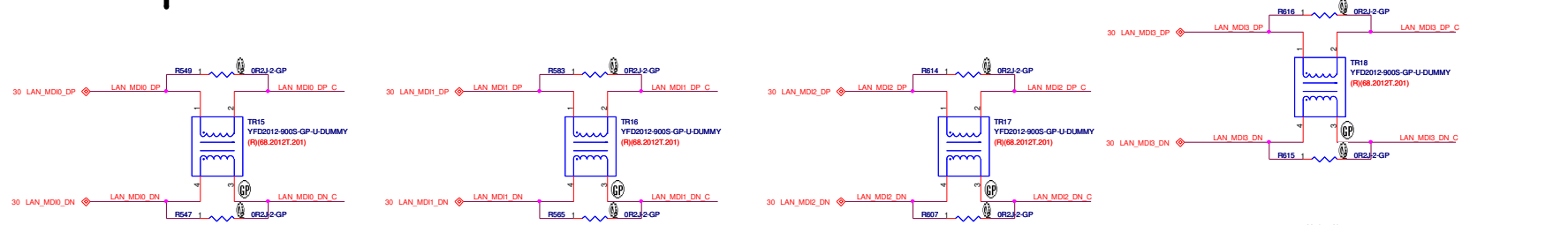
```

```

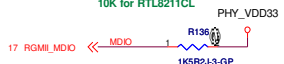
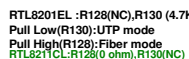
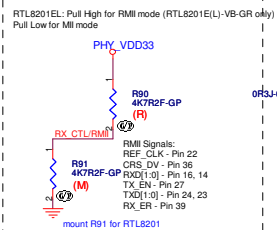
30 LAN_LINK_100 >>
30 LAN_LINK_1000 >>
30 LAN_LED_LINK >>

30 LAN_MDIO_DN << LAN_MDIO_DN
30 LAN_MDIO_DP << LAN_MDIO_DP
30 LAN_MDIO_DN << LAN_MDIO_DP
30 LAN_MDIO_DP << LAN_MDIO_DP
30 LAN_MDI_DN << LAN_MDI_DN
30 LAN_MDI_DP << LAN_MDI_DP
30 LAN_MDIO_DN << LAN_MDIO_DN
30 LAN_MDIO_DP << LAN_MDIO_DP

```

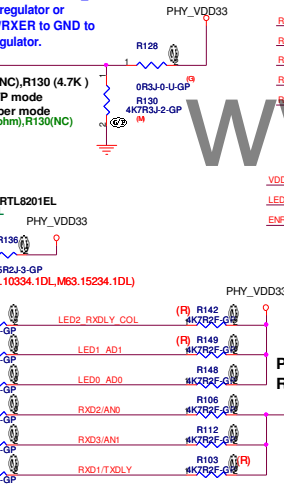


RTL8211CL Giga LAN
RTL8201EL 10/100 LAN



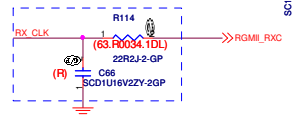
RTL8201EL:
R69:MII Interface
R70:SNI Interface
R71,R74: PHY Address=11

RTL8211CL:
R76,R78: Config for all capability
R71,R74: PHY Address=11
R69,R85: Without TX/RX Delay

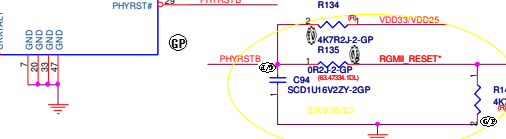


Close to PHY for 8201EL
Reserve for EMI

**Place filter network close to RX_CLK.
Reserved for EMI**

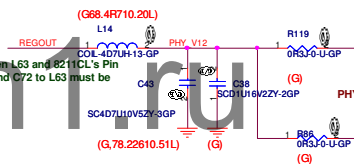


Note 2: The Trace length from C63, C325 to 8211CL Pin 44,45 must be within 1 cm. The trace width from PHY_AVDD33 to Pin 44,45 should>40mils

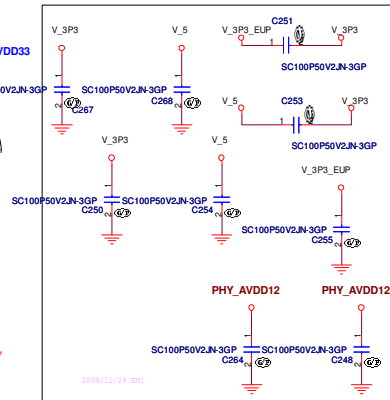
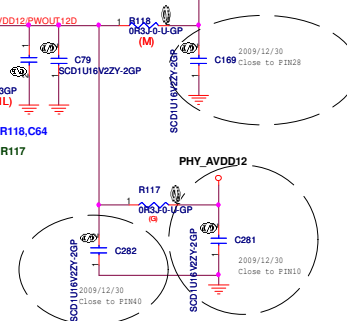
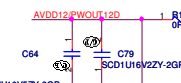
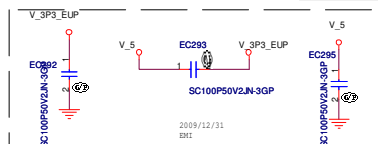
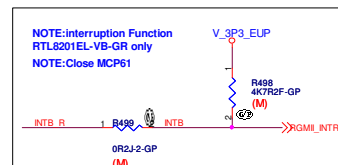


For RTL8211CL


Note 1: The Trace length between L63 and 8211CL's Pin 48 must be within 0.5 cm. C40 and C72 to L63 must be within 0.5cm.



RTL8201EL:R105(NC)
RTL8211CL: R105 for 3.3V RGMII



<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
88E1116R GBIT LAN			
Size	Document Number	Rev	
Custom	eMaguire	1M	
Date:	Thursday, February 11, 2010	Sheet	36 of 46

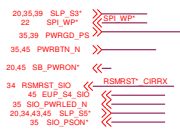
LPC



FAN



Sequence

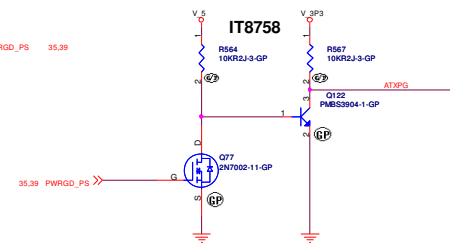
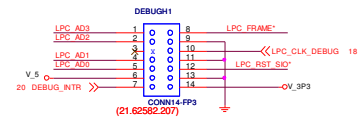
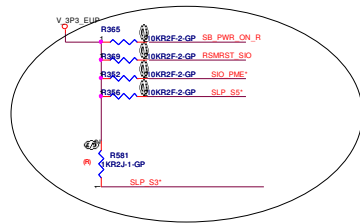
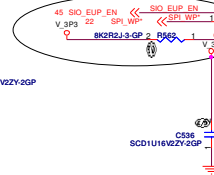
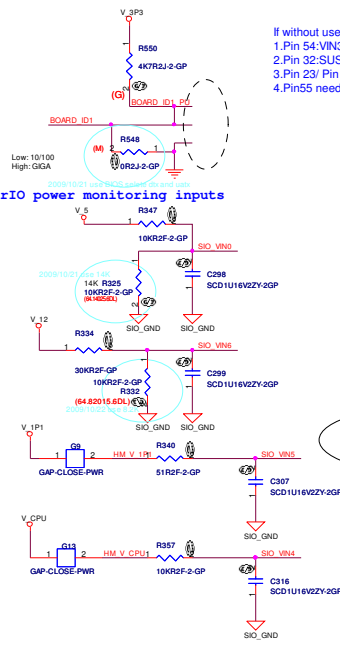


KB/MS

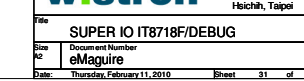
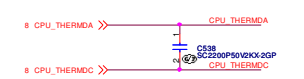
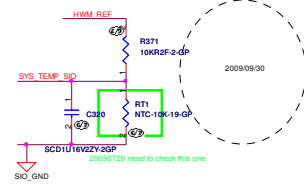


If without use these pins, Please pull-up to VCC. Don't let it floating
 1. Pin 54-VIN3/ATXPG
 2. Pin 32-SUSB#
 3. Pin 23/ Pin 58/ Pin 60/ Pin 62
 4. Pin55 need 2.8V

SuperIO power monitoring inputs



2009/09/21

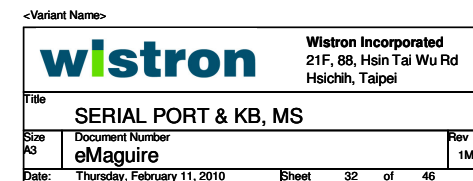


www.aitech1.ru

31 SIO_KCLK >>_____

31 SIO_MDAT <<>>_____

31 SIO_MCLK >>_____



Delete LPT Port

www.aitech1.ru

<Variant Name>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

PARALLEL PORT/HEADER

Size
A3

Document Number
eMaguire

Rev
1M

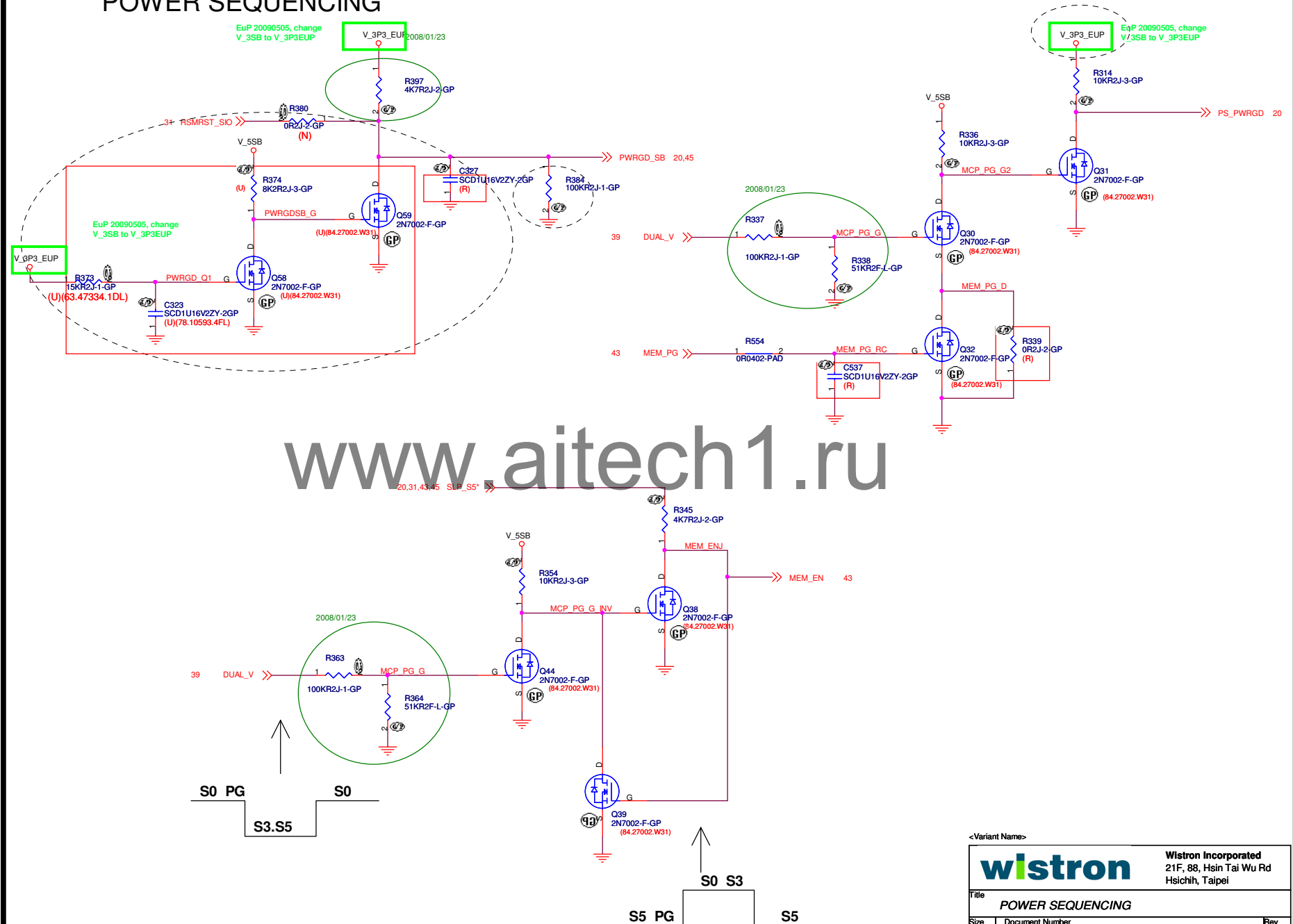
Date: Thursday, February 11, 2010

Sheet 33 of 46

Sequence

20,45 PWRGD_SB <<
 39 DUAL_V >>
 43 MEM_PG >>
 20 PS_PWRGD <<
 43 MEM_EN <<
 20,31,43,45 SLP_S5* >>

POWER SEQUENCING



www.aitech1.ru

<Variant Name>

wistron

Wistron Incorporated
 21F, 88, Hsin Tai Wu Rd
 Hsichih, Taipei

Title

POWER SEQUENCING

Size

Document Number

A3

eMaguire

Rev

1M

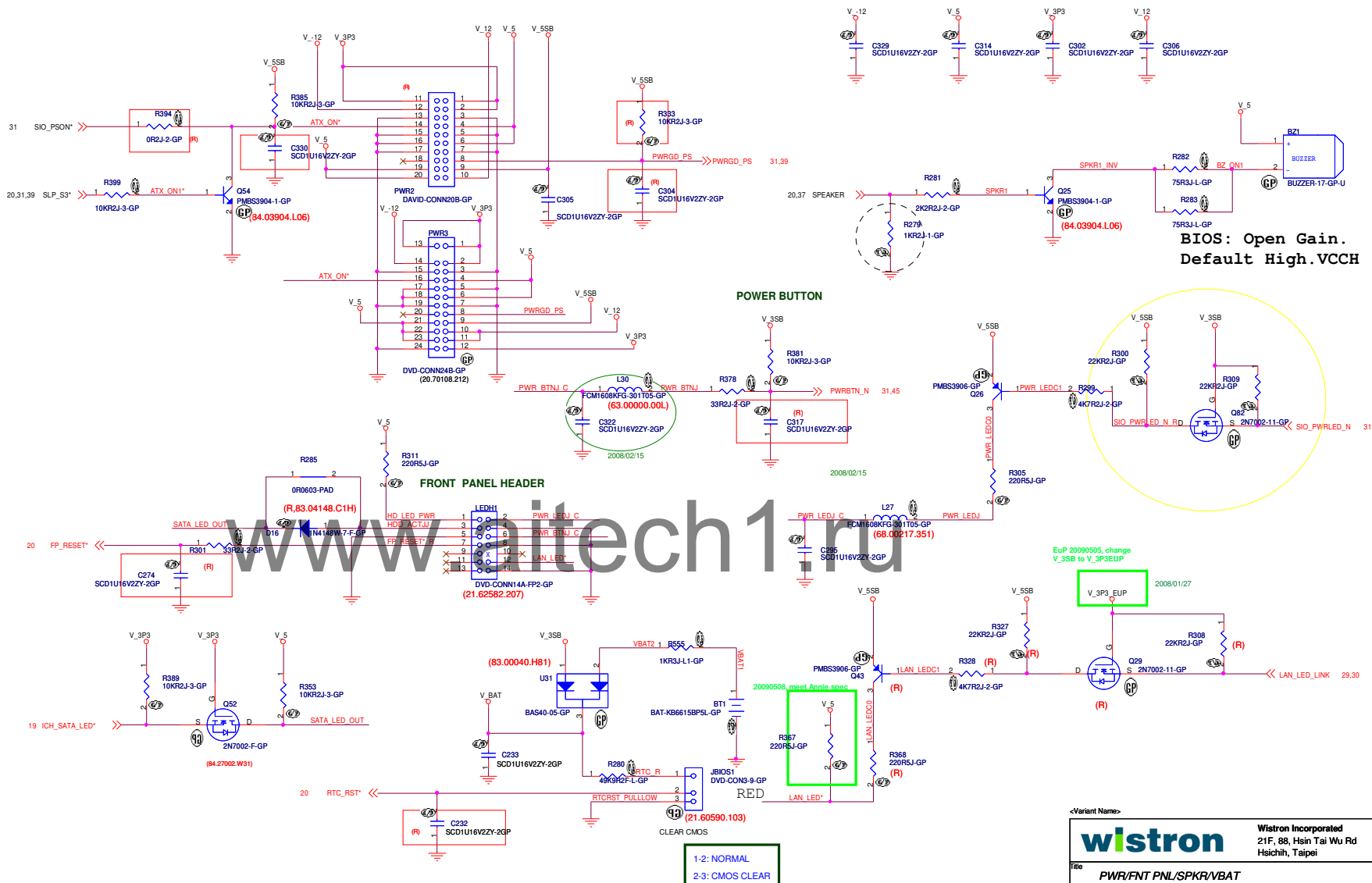
Date: Thursday, February 11, 2010


Sheet 34 of 46

Sequence

31 SIO_PSON* >> _____
 20,31,39 SLP_S3* >> _____
 31,39 PWRGD_PS << PWRGD_PS
 20,37 SPEAKER >> _____
 31 SIO_PWRLED_N >> _____
 31,45 PWRBTN_N << _____
 29,30 LAN_LED_LINK >> _____
 20 RTC_RST* << _____
 20 FP_RESET* << _____
 19 ICH_SATA_LED* >> _____

ATX CONNECTOR



<Variant Name>			
		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title		PWR/FNT PNL/SPKR/VBAT	
Size	Document Number	Rev	
Cust	Maguire	1M	
Date:	Thursday, February 11, 2010	Sheet	35 of 46

```

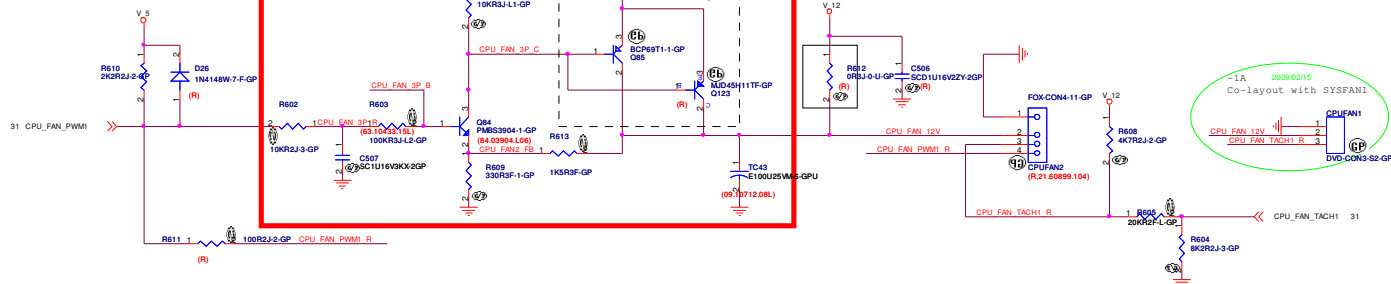
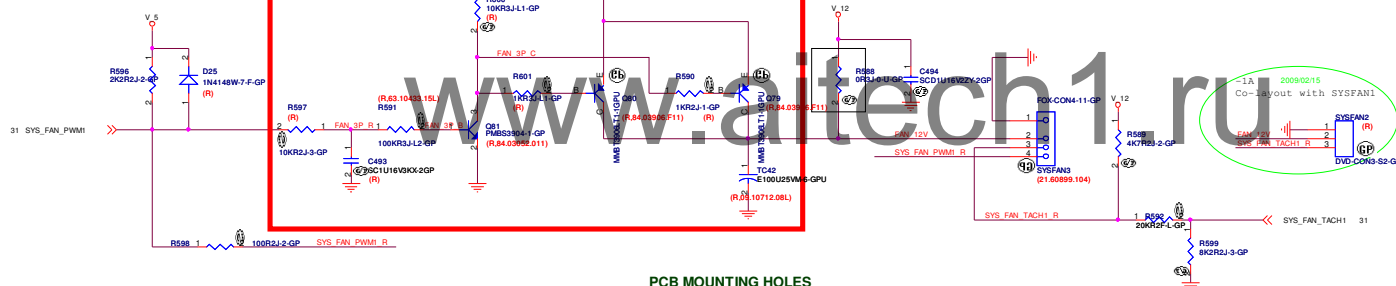
31 CPU_FAN_PWM1
31 CPU_FAN_TACH1

```

```

31 SYS_FAN_PWM1
31 SYS_FAN_TACH1

```

[illegible][illegible]

HDA

20,22 HDA_SDOU
20 HDA_SDI0

20,38 HDA_RST*
20 HDA_SYNC
20 HDA_BITCLK

AUDIO

20,35 SPEAKER <<SPEAKER>>

38 SPDIF_OUT1 << >>
38 AUD_IN_L << >>
38 AUD_IN_R << >>

38 AUD_MIC1_L << >>
38 AUD_MIC1_R << >>
38 MIC1_VREF0_R << >>
38 MIC1_VREF0_L << >>

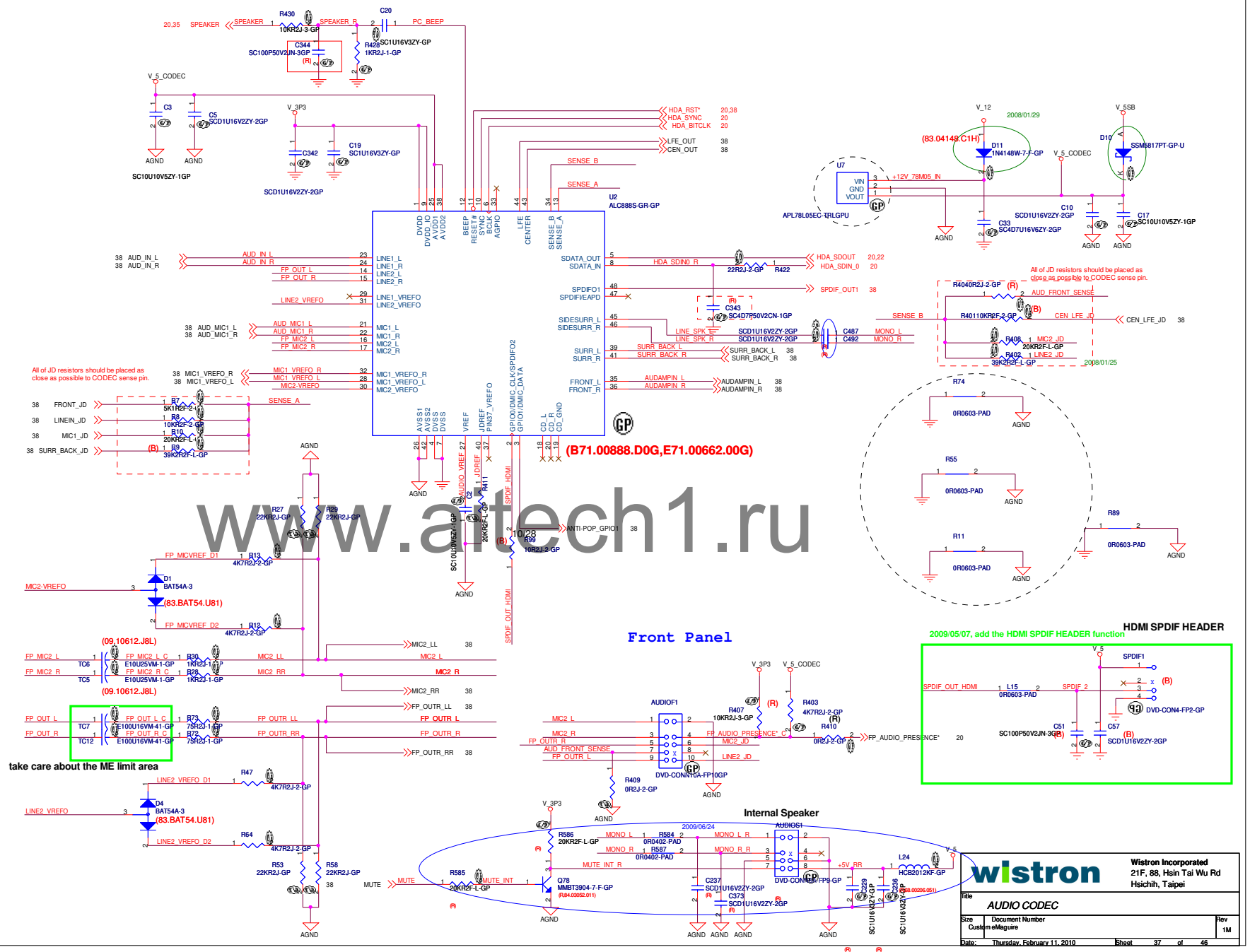
38 FRONT_JD << >>
38 LINEIN_JD << >>
38 MIC1_JD << >>
38 SURR_BACK_JD << >>

38 MIC2_LL << >>
38 MIC2_RR << >>
38 FP_OUTR_LL << >>
38 FP_OUTR_RR << >>

38 ANTI-POP_GPIO1 << >>
38 SURR_BACK_L << >>
38 SURR_BACK_R << >>

38 AUDAMPIN_L << >>
38 AUDAMPIN_R << >>
38 CEN_LFE_JD << >>

38 LFE_OUT << >>
38 CEN_OUT << >>
20 FP_AUDIO_PRESENCE* << >>

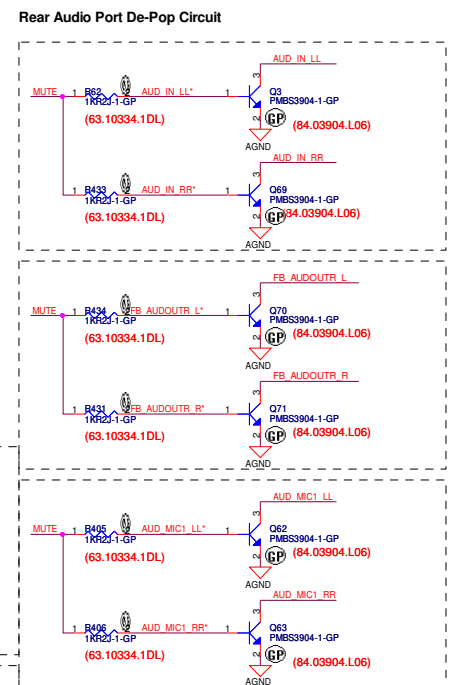
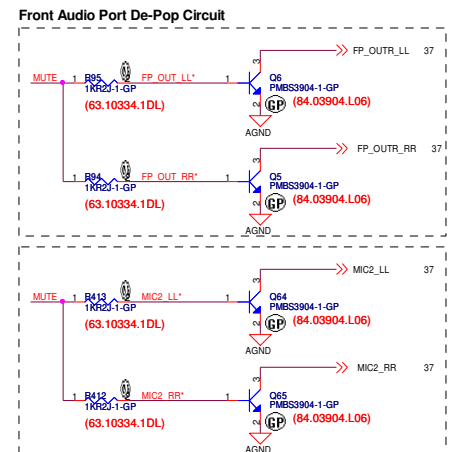
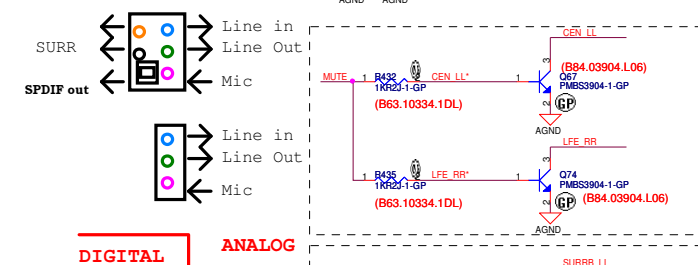
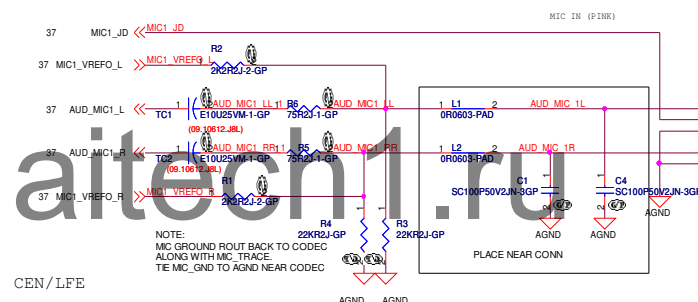
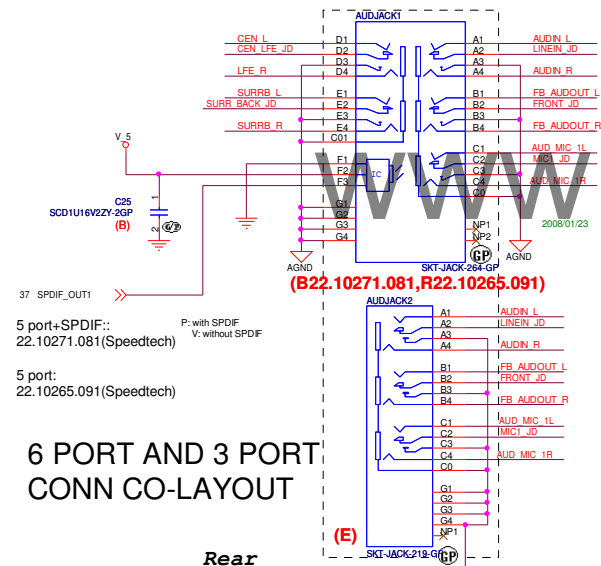
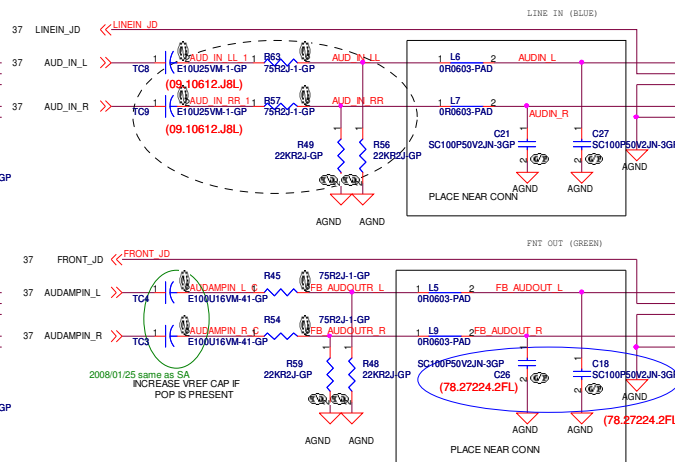
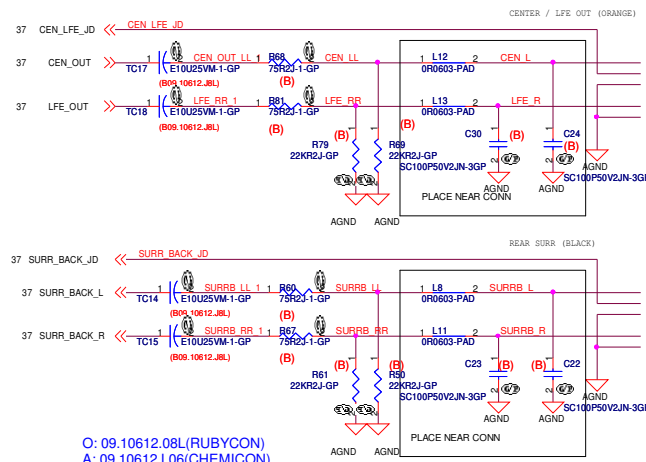


```

37  CEN_LFE_ID  << CEN_LFE_ID
37  CEN_OUT  >> _____
37  LFE_OUT  >> _____
37  SURR_BACK_ID  << SURR_BACK_ID
37  SURR_BACK_L  << _____
37  SURR_BACK_R  << _____
37  SPDIF_OUT1  >> _____
20,37  HDA_RST*  >> _____
37  ANTI-POP_GPIO1  >> _____

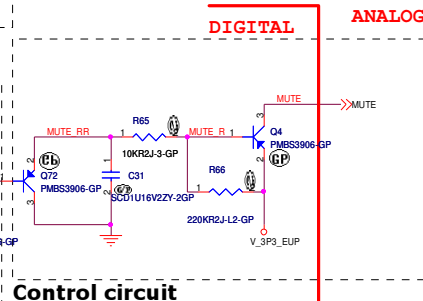
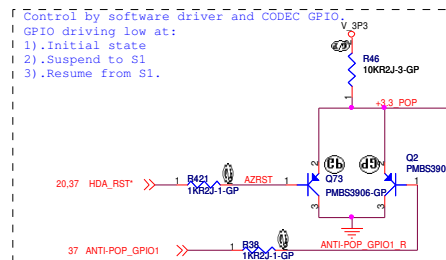
LINEIN_ID  << LINEIN_ID
37  AUD_IN_L  >> _____
37  AUD_IN_R  >> _____
37  FRONT_ID  << FRONT_ID
37  AUDAMPIN_L  >> _____
37  AUDAMPIN_R  >> _____
37  MIC1_ID  << MIC1_ID
MIC1_VREF0_L  >> MIC1_VREF0_L
37  AUD_MIC1_L  << _____
37  AUD_MIC1_R  << _____
MIC1_VREF0_R  >> MIC1_VREF0_R
37  FP_OUTR_LL  >> _____
37  FP_OUTR_RR  >> _____
37  MIC2_LL  >> _____
37  MIC2_RR  >> _____

```

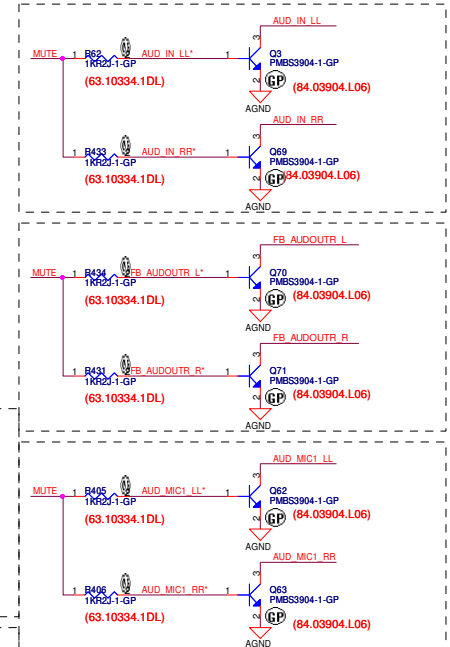


POP Circuit

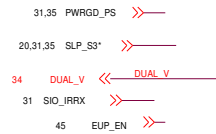
```
Control by software driver and CODEC GPIO
GPIO driving low at:
1).Initial state
2).Suspend to S1
3).Resume from S1.
```



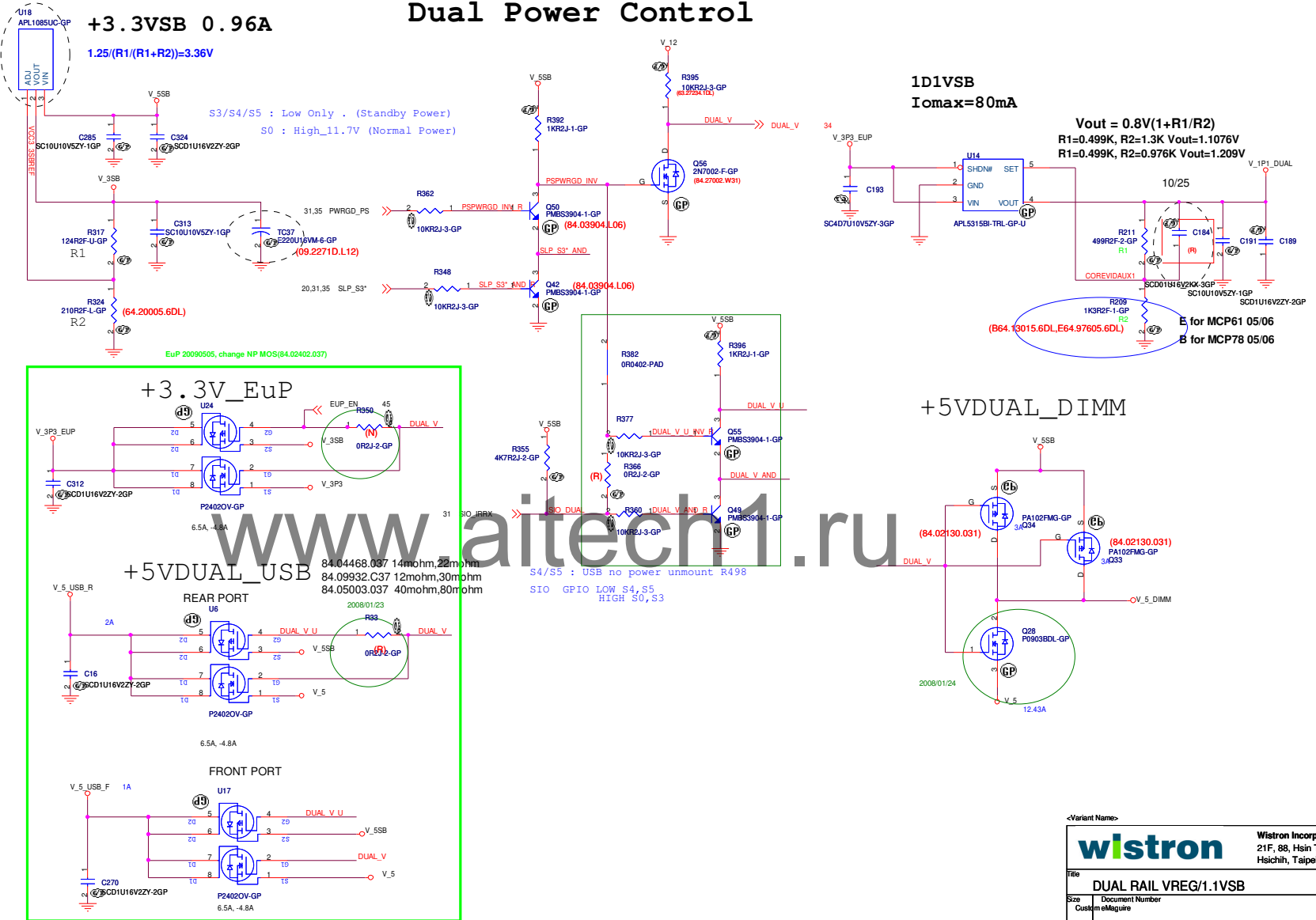
Rear Audio Port De-Pop Circuit



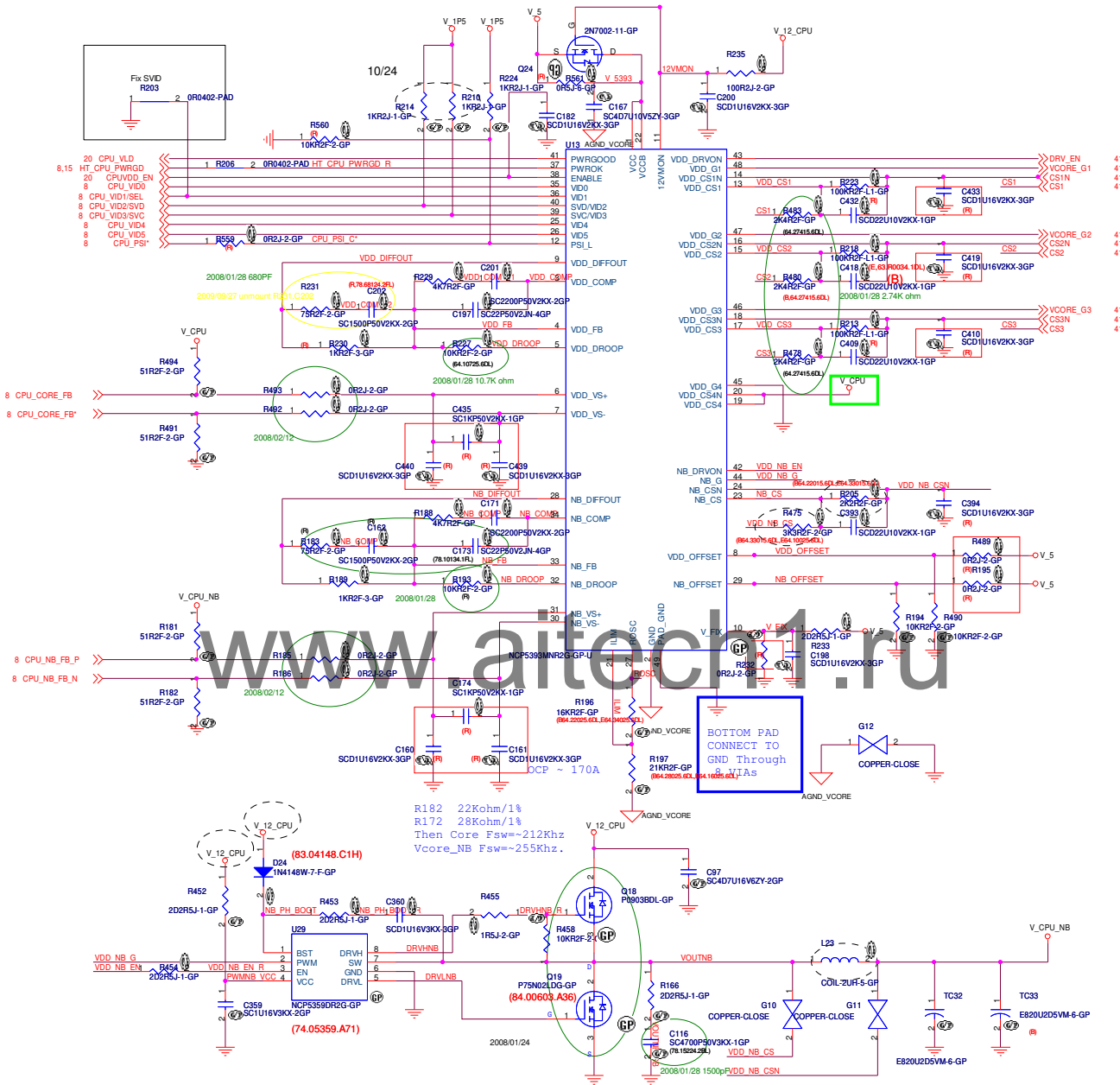
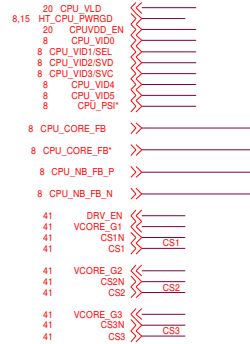
Sequence



Dual Power Control



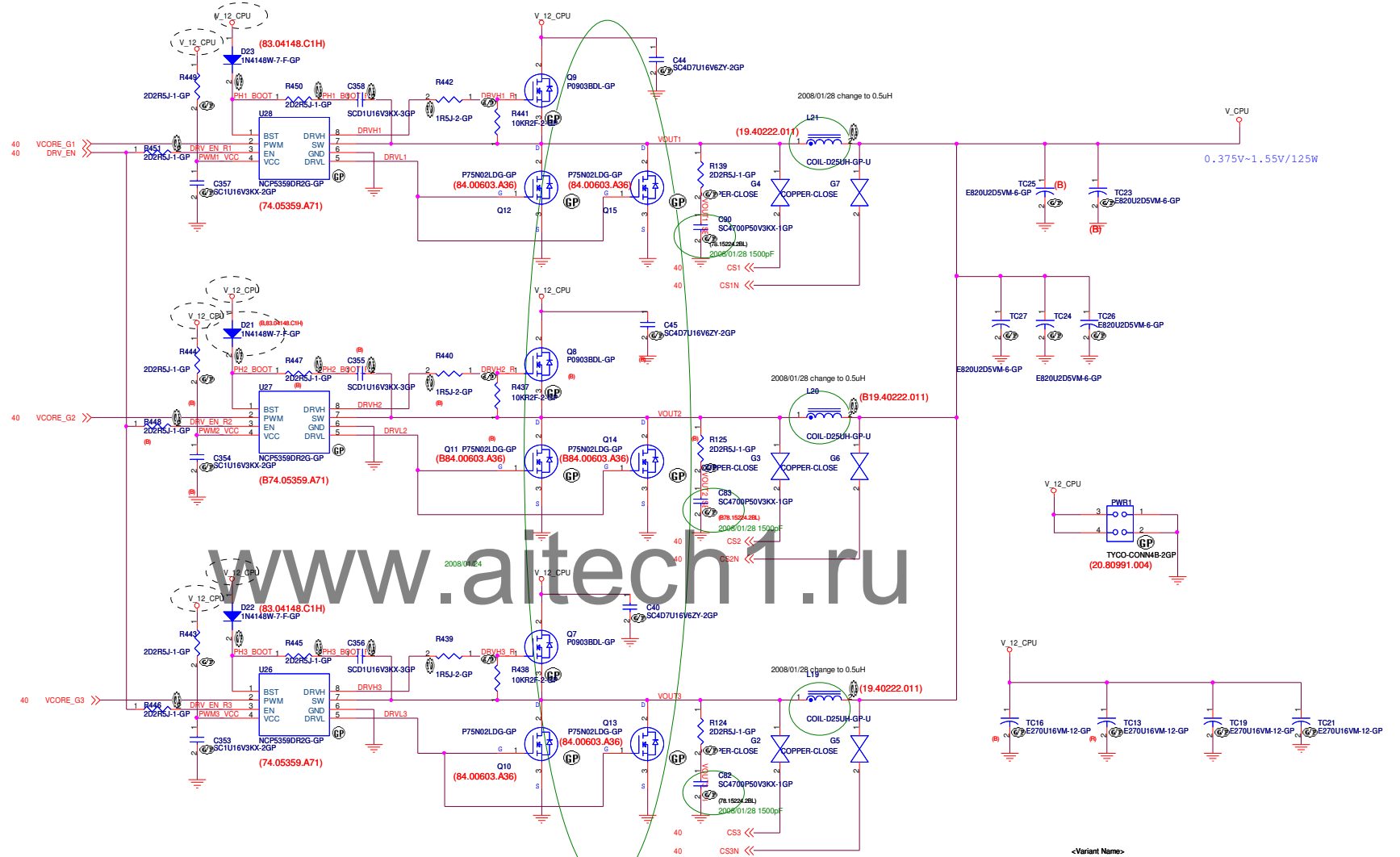
VCORE PWM



<Variant Name>		
wlstron		
Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
Title NCP5393 CONTROL		
Size Customer	Document Number Maguire	Rev 1M
Date: Thursday, February 11, 2010	Sheet 40	of 46

VCORE PWM

40 VCORE_G1 >>>
40 VCORE_G2 >>>
40 VCORE_G3 >>>
40 CS1 <<<
40 CS1N <<<
40 CS2 <<<
40 CS2N <<<
40 CS3 <<<
40 CS3N <<<

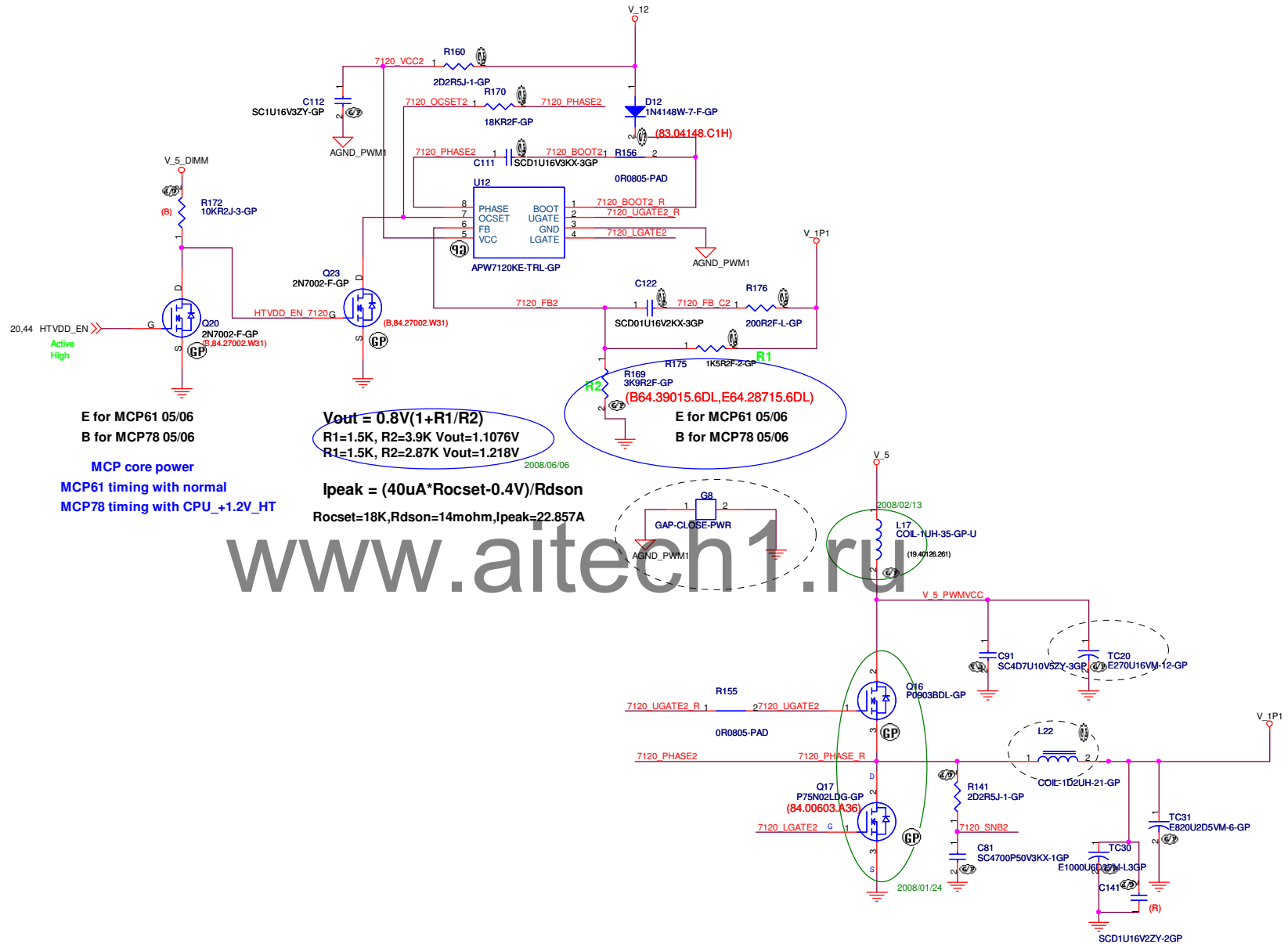


<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
File NCP5393 PHASE 1, 2, 3			
Size	Document Number	Rev	
Customer	Maguire	1M	
Date:	Thursday, February 11, 2010	Sheet	41 of 46

MCP PWM

20,44 HTVDD_EN



<Variant Name>

wistron

Wistron Incorporated
 21F, 88, Hsin Tai Wu Rd
 Hsichih, Taipei

Title
APW7120 1.1V

Size A3 Document Number eMaguire Rev 1M

Date: Thursday, February 11, 2010 Sheet 42 of 46

MEM PWM

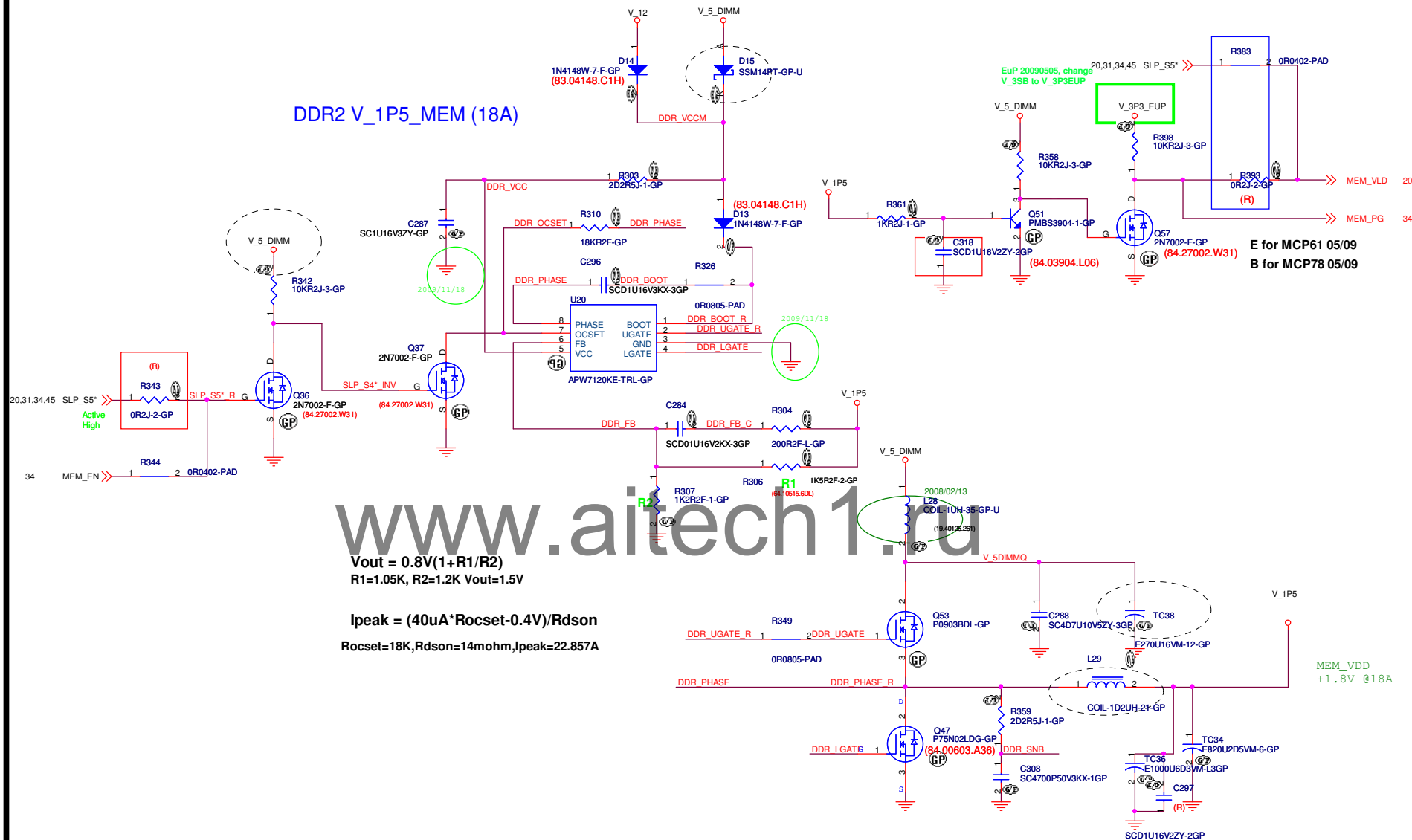
20,31,34,45 SLP_S5* >>>

34 MEM_EN >>>

20 MEM_VLD <<<

34 MEM_PG <<<

DDR2 V_1P5_MEM (18A)




HT_VLD <<—

2 HTVDD_EN >>—

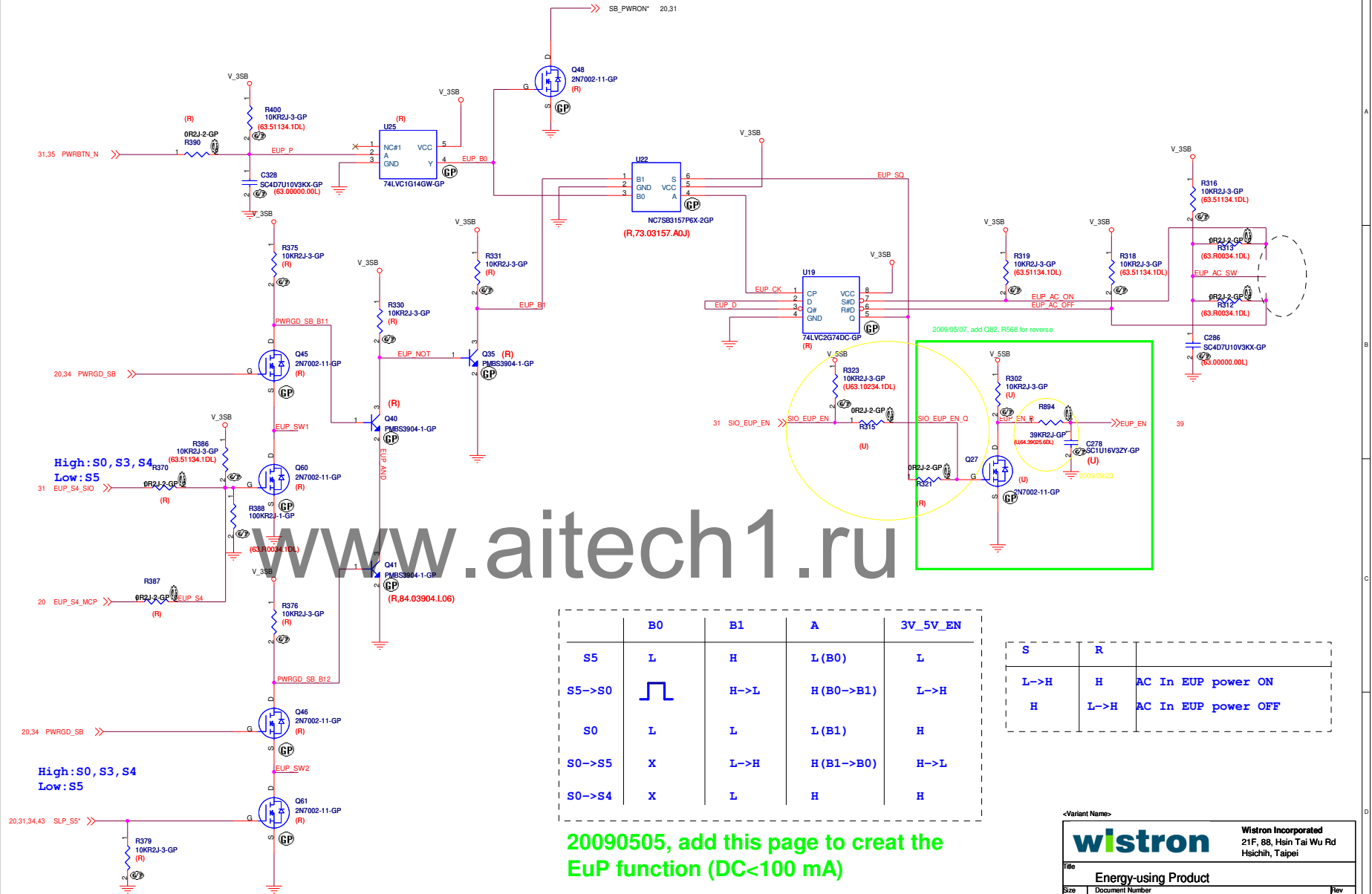
20 HT_VLD <<—

20,42 HTVDD_EN >>—

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
.LDO FOR 2.5V/1.2V/0.9V			
Size A3	Document Number eMagure	Rev 1M	
Date: Thursday, February 11, 2010	Sheet 44	of 46	

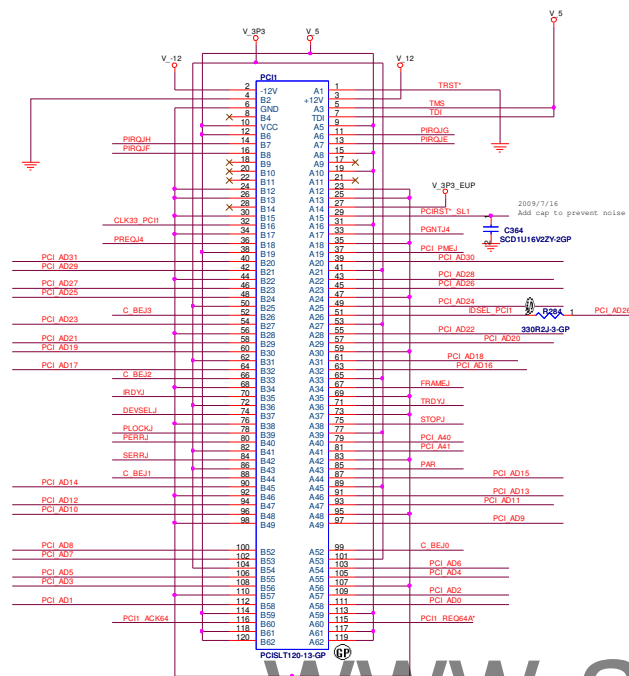
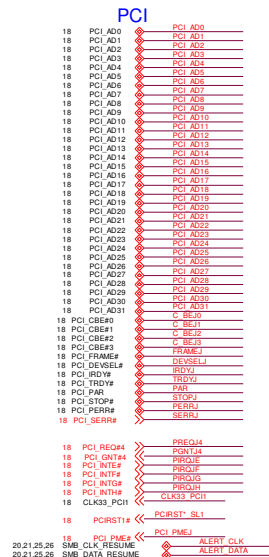
EUP

31,35 PWRBTN_N >>
 20,34 PWRGD_SB >>
 31 EUP_S4_SIO >>
 20 EUP_S4_MCP >>
 20,34 PWRGD_SB >>
 20,31,34,43 SLP_S5* >>
 20,31 SB_PWRON* <<
 39 EUP_EN <<



20090505, add this page to creat the EuP function (DC<100 mA)

20090506 chane all V_5SB to V_3SB in this page



INTG#, INT#H#, INT#E#, INT#F#

REQ#4#, GNT#4#

IDSEL1: AD26

